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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a display means for displaying a dot matrix and a method for displaying information.

Related Background Art

The EP-A-0 300 509 discloses a character and graphics display device for displaying character and graphics data comprising a receiving circuit for deriving the character and graphics data from a signal carrying that data encoded therein, a memory for storing the received data, a decoder circuit for decoding the encoded data into suitable form for transfer to a display device, a display memory for temporarily storing this decoded data, and compression circuits for converting the decoded data into a form whereby patterns represented by that data are displayed in compressed size. Thus, pattern and graphics data can be displayed together with other data such as a television picture or a number of pages of the character and graphics data can be displayed simultaneously.

Furthermore, electronic devices such as electronic notebook, word processor or personal computer using a liquid crystal or plasma display as display means are well known, in which so-called automatic power off control is often used where if there is no input such as an operational instruction for a predetermined time, the power supply is turned off for a display unit or the whole electronic device to save the power.

However, in the electronic devices as above described, when it is desired to think while watching the screen without input for a certain time, or watch the information displayed on the screen at times, it is very incovenient that the screen disappears in a fixed time.

Also, in the type of automatically turning off the power of the whole device, the operation must be restarted from the beginning by turning on the power, which will take some labor and time.

On the other hand, in the type of stopping only the screen display, such a problem may not arise in that an original screen can be restored by the keyboard operation, but there was a disadvantage that a person except for the operator could not know the operation state of the device or the on/off state of power supply.

However, such a method may be very inconvenient when it is desired to think while watching the screen without input such as an operational instruction for a certain time, or watch the information displayed on the screen at times. Also, in the type of automatically turning off the power supply of the whole device, there is a trouble that to operate the device again after turning the power off, the operation from the power on to the display of necessary screen must be performed again. The device in which only the screen is turned off can restore the screen with the input from the keyboard, but there was a problem that the operation state of the device or the on/off state of power supply could not be known to a person except for the user, only by baking a glance at the screen, while the screen was being turned off.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a display means as well as a respective method which overcome the above-mentioned problems and which allow the power-saving consistently with the visibility of the display and the operativity of the device by performing an appropriate display control.

This object is achieved by the display device according to the claim 1 and the method according to the claim 8, respectively.

Thus, it is possible to reduce the display area for use in driving the display in accordance with a desired control condition, and to display compressed image data within the reduced display area.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a liquid crystal controller for switching between the normal mode and the reduction mode.
Figs. 2A and 2B are timing charts in the normal mode and the reduction mode, respectively.
Fig. 3 is a block diagram for a liquid crystal display driver.
Figs. 4A and 4B are explanation views for showing the weighting process in the reduction and smoothing control.
Fig. 5 is a flowchart for the reduction and smoothing control.
Figs. 6A to 6D are explanation views for exemplifying the screen display.
Fig. 7 is a perspective view showing the appearance of an electronic device.
Fig. 8 is a block diagram for the whole of a control system in the electronic device.
Fig. 9 is a block diagram showing a constitution using an active matrix liquid crystal.

Fig. 10 is a block diagram for a reduction and smoothing hardware.
Fig. 11A is a timing chart for the display in the normal mode.
Fig. 11B is a timing chart for the display in the reduction mode.
Figs. 12-1A and 12-1B are views exemplifying the display of a universal clock screen.
Figs. 12-2A and 12-2B are views exemplifying the dispaly of an address screen.
Figs. 12-3A and 12-3B are views exemplifying the display of an address screen.
Figs. 12-4A and 12-4B are views exemplifying the display of a calendar screen.
Figs. 12-5A and 12-5B are views exemplifying the display of a schedule screen.
Figs. 13-1A nad 13-1B are views exemplifying the display of a screen.
Figs. 13-2A and 13-2B are views exemplifying the display of a screen.
Fig. 14 is a flowchart for constituting a screen in the reduction mode.
Figs. 15A and 15B are views exemplifying the display of a screen with the user specification.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described below based on the examples as shown in the drawings.

An external view of a personal information device by the use of the present invention is shown in Fig. 7.

As shown in the figure, the personal information device of this example is one of inputting a character command on an input/output plane 31 in a combination of a transparent digitizer and a liquid crystal panel, with the handwriting by means of an input pen 30, and displaying a pen locus, a result of character recognition or a result of application.

A block diagram for the whole control system of the device of Fig. 7 is shown in Fig. 8.

The control system of Fig. 8 is to control the whole operation of the device with a CPU 19 having a microprocessor. A system bus of the CPU 19 has connected to each member as shown. In the following, each member will be described.

In a ROM 20 is stored a control program for the CPU 19 (and application programs, OS, and dictionary data, in addition to a procedure as shown in Fig. 5), while a RAM 21 is used for a work area of the CPU 19 or a RAM disk area.

Numerals 22 to 24 show interface circuits for an IC (memory) card as external storage means, a serial port such as RS232C, and a centronics port (i.e., a parallel port mainly for the printer), respectively.

An input/output plane 31 as shown in Fig. 7 is a combination of a transparent digitizer and a liquid crystal panel, which are indicated by numerals 25 and 17, respectively.

The display of the liquid crystal panel 17 is controlled via a liquid crystal controller/driver 18. The display data is stored in a VRAM 10. The transparent digitizer 25 is constituted of a digitizer of the resistive film method in which two sheets of glass (or one sheet of PET and the other of glass) with a resistive film deposited are opposed and the voltage at the time when two sheets of resistive film are contacted with the pressure of a pen is converted into a coordinate.

The input or output into or from the transparent digitizer 25 is controlled via a digitizer driver for obtaining the input coordinate with an input pen, and an A/D converter for converting the digitizer voltage into a digital value.

The power for the device is supplied from a power source unit 28 composed of a battery or a switching power source.

The application of such an information device (which is supplied by being stored in the ROM 20 or by the use of a medium such as an IC card) may be①universal clock,②schedule,③address note, and④character, calculation or drawing note.

Fig. 1 shows a constitution of the liquid crystal controller/driver 18 as shown in Fig. 7 for essential parts thereof.

A circuit of Fig. 1 reads display data from the VRAM 10 and transfers them to a driver (Fig. 3), as well as issuing a control signal, but this example is particularly provided with a reduction mode of reducing the display range of a display unit to decrease the transfer frequency of control signal and data, in addition to a normal mode.

Here, the liquid crystal panel 17 is a matrix liquid crystal of 320x128 dots, for example, with its display data being stored in the VRAM 10.

In the figure, numeral 1 is a frequency divider and frequency selector constituted of a counter and a selector, in which an input clock (e.g., 667KHz) and a 1/4 frequency-divided clock (e.g., 167KHz) are selected by frequency select signal set in a register 2, and output as a line counter 3, a total counter 6 and a liquid crystal clock CP.

In the reduction mode of input clock, the clock having a quarter of the frequency in the normal mode is selected. The line counter 3 and the register 4 are to set the timing of a load signal LOAD, in which the setting is made so that the load signal is issued once for 80 clocks (320 dots) in the normal mode, or once for 40 clocks (160 dots) in the reduction mode.

The setting value for the register 4 is written by the CPU. A load timing controller 5 adjusts the signal width from a count-up signal of the line counter 3, and outputs it as the load signal LOAD. The load signal LOAD is a signal for latching one line of data transmitted to the liquid crystal driver (Fig. 3).

A frame signal FRAME and an address B for VRAM data access are created by the total counter 6 and the register 7. As the liquid crystal screen has 320x128 dots in the normal mode of this example, the frame is generated one for every 128 lines. The number of counts for the register 7 is set by the CPU 19.

A frame signal controller 8 generates a signal DF for reversing the bias polarity of liquid crystal for each one frame, as well as outputting the frame signal FRAME at the timing when the total counter 6 counts up.

The number of counts in the total counter 6 directly becomes an address (address B) for accessing the VRAM 10.

An image data in the VRAM 10 is read and written through a liquid crystal data controller 9. When the CPU 19 reads or writes the content of the VRAM 10, the address A is selected, or when it reads the display content into the liquid crystal driver, the address B is selected, in which both timings are controlled not to be overlapped with each other.

As the data read from the VRAM 10 is 8 bits, and 4-bit data is transferred to the liquid crystal driver, read data is divided into upper and lower 4 bits which are sent out synchronously with the clock (CP).

The signals DISP OFF1 and DISP OFF2 set in the register 2 are control signals for turning the display of the liquid crystal driver into the OFF state (constant output voltage), in which in the normal mode, these signals DISP OFF1 and DISP OFF2 are turned into "H" in all the drivers, while in the reduction mode, only the DISP OFF1 which is connected to unused drivers is turned into "L".

The timing waveforms of the operation as above described are shown in Figs. 2A and 2B. Fig. 2A is in the normal mode, and Fig. 2B is in the reduction mode. The waveform is represented in one frame with the signals LOAD, DF and FRAME as shown in the upper portion, and in one line with the signals DF to address B as shown in the lower portion. In Figs. 2A and 2B, the time width corresponding to one frame is the same.

Fig. 3 shows a drive circuit of liquid crystal panel 17. 11 and 12 are command drivers (e.g., MSM5298: Oki Electric Industry Co.), and 13, 14, 15 and 16 are segment drivers (e.g., MSM5299: Oki Electric Industry Co.). In the normal mode, all the drivers are used, while in the reduction mode, the drivers 11, 13, 14 are used.

Accordingly, the signal DISP OFF2 is connected to the drivers 11, 13, 14, and the signal DISP OFF1 is connected to the drivers 12, 15, 16.

Next, the reduction and smoothing of the display screen will be described with reference to Figs. 4A and 4B. Each square as shown in Figs. 4A and 4B indicates one display dot on the liquid crystal panel 17.

In the reduction of display image in this example, 4 dots are converted into one dot to reduce the screen by half, and the smoothing is performed to decrease the spatial frequency of image to decrease the apparent frequency for transfer of data.

Thus, 12 dots of pixel (a5 to a16) around 4 dots of pixel of interest (a1 to a4) are picked up as shown in Fig. 4A, and the weight is given to each pixel as shown in Fig. 4B.

The pixel of interest is largest and the pixel is made smaller on the diagonal. If the value A obtained according to the following expression is $A \geqq 19$, the dot for that pixel of interest is made "H", while if $A < 19$, it is made "L" ($A=36$ for all black pixels).

$$A = 4\sum_{n=1}^{4} an + 2\sum_{n=5}^{12} an + \sum_{n=13}^{16} an \quad \cdots (1)$$

Next, a control procedure for performing the reduction and smoothing of Figs. 4A and 4B with a software is shown in a flowchart as shown in Fig. 5. The procedure as shown is executed by the CPU 19. Note that in the procedure of Fig. 5, the area for display data is assigned to a region of the VRAM 10 or RAM 21 as VRAM1 and VRAM2.

At step S1 of Fig. 5, the pixel of interest and peripheral data are read from the VRAM 10 in which the information of currently displayed image is stored. As the 8-bit reduced image data is created at one time of reading, the data is constituted of a total of 16 bytes which are 4 bytes as the pixel of interest and 12 bytes as the peripheral pixel. Note that data at the end portion without image is made zero.

At step S2, the data read at step S1 is decomposed into bit data a1 to a16 for each pixel of interest, and at step S3, each pixel element (a1 to a16) is given the weight according to the expression (1) to calculate the value of A.

At step S4, it is determined whether the reduction and smoothing result for the pixel of interest is 1 or 0, depending on whether or not the calculated value A is greater than or equal to 19. At step S4, if A is greater than or equal to 19, the procedure proceeds to step S5, where the pixel of interest is set to 1 or "black", or if it is less than 19, the procedure proceeds to step S6, where the pixel of interest is set to 0 or "white".

And at step S7, one bit for the pixel of interest is converted into byte data sequentially in accordance with the image position.

At step S8, it is determined whether or not the data for the pixel of interest is calculated with 8 bits, and if not, the procedure returns to step S2 again, where the next pixel of interest is calculated in the same way. When calculated with 8 bits, the data is written into the VRAM1 which is a buffer for reduced data.

If the data conversion for one frame has not been completed at step S10, the procedure returns to step S1 again, where the next group of 16 bytes for the pixel of interest is read and the calculation is continued.

If one frame has been completed, data of the VRAM 10 is saved into the VRAM2, at step S11, and the data of the VRAM1 is transferred to the VRAM10, at step S12. Thereby, the image displayed on the screen of the liquid crystal

panel 17 can be reduced and smoothed.

Note that this mode is entered automatically when there is no input by the user for a predetermined period (e.g., five minutes) or if the mode is set by the user, although the subsequent flowchart is not shown.

And if there is any input by the user, original image saved in the VRAM2 is immediately transferred to the VRAM to return to the normal screen mode. In the application where the display screen is required to change its value also in the reduced screen like the clock, a time display portion is reduced and smoothed according to the algorithm as previously described, and written into the VRAM 10.

The reduction and smoothing process of display screen as above described can be executed, instead of the conventional automatic power off control, when it is confirmed that there is no input for a fixed period with a well-known method of measuring the time interval by an input pen 30, and in addition, can be performed in accordance with a user instruction with the input pen 30 or a switch operation, not shown.

If the display screen is represented in the reduction and smoothing, with the transfer frequency for display data and control signal decreased, and the display driver unit not contributing to the display turned off, the electric power for use in connection with the display can be greatly saved while the information required by the user always appears on the screen.

And the reduction is not simply performed by thinning out the dot, but along with the smoothing process, the high quality of image can be displayed, without damaging the visibility of display and operativity.

Also, in the conventional method in which the whole display is erased, there was a problem that the state of device could not be judged only by a visual inspection of device, but this example does not have such a problem.

Note that the input control and the time measurement other than the display can be also normally performed in the reduced screen.

Here, examples of the screen display in typical applications of the electronic device in this example are shown in Figs. 6A to 6D.

The display of Fig. 6A is a universal clock, in which the year, month and day appearing in the central position indicates Japanese standard time. This is such an application that if each site in a world map is pointed to with a pen (with the display screen integral with a digitizer) or mouse, the standard time of each site is indicated.

If the above-mentioned reduction and smoothing process is applied to the display of this application, the display reduced to 1/4 in the area ratio can be obtained as shown in Fig. 6B.

The reduced image has a part of the map disappeared by the smoothing, but with the above-mentioned smoothing processing, the day and time can be read.

On the other hand, a calendar of Fig. 3 is an application in which the schedule for a specified day can be registered and confirmed by pointing to that specified data. With the above-mentioned smoothing process, the reduced screen has the ruled line and the day of week for the calendar disappeared, but the characters representing the day, or year and month can be read (Fig. 6D).

While in the above example, a simple matrix method was explained as the driving method by supposing the liquid crystal as the display element, an active matrix method using amorphous Si, polycrystalline Si or thin film transistor (TFT) will be described below as the driving method of the liquid crystal.

The active matrix method has one transistor for one pixel arranged on a substrate, and is also effective for the representation of half tone.

As shown in Fig. 9, the matrix structure is constituted by a scanning circuit and a data driver circuit, in which in the reduction mode, as previously described, the scanning circuit 91 is changed from the scanning of terminals 1 to 80 of the active matrix to that of terminals 1 to 40, with the clock frequency made half, and further, the supply of display data via the data driver 92 is changed from the full use of terminals 1 to 320 to that of terminals 1 to 160, so that the reduced screen and the power-saving can be accomplished.

It is of course possible that other than the liquid crystal display, the same control can be made by using a simple matrix, EL (electronic luminescence) of active matrix or a plasma display.

In the example as previously described, the compression and smoothing was made with the software based on the expression (1), but can be also made with the hardware. Fig. 10 shows one example of such a hardware configuration. A circuit of Fig. 10 performs mainly the weighting process as previously mentioned with the hardware.

In Fig. 10, numerals D1 to D16 are shift registers, in which pixel data input in 4-bit parallel into the terminals A to E are given the weights, respectively, and added in an adder circuit 94, and then it is determined by a comparator 95 whether or not an addition result is greater than or equal to 19, whereby an output data F of one byte can be obtained. If the data of A to E is shifted by 2 bits every time on bit is obtained, compressed data F of eight bits can be obtained.

The weighting is not limited to that as shown in Figs. 4A and 4B, but it is of course possible that other coefficients can be adopted in accordance with a desired display control condition.

As will be clearly understood, according to the present invention, an electronic device having display means for displaying a dot matrix is constituted by comprising means for variably controlling the number of lines or rows for actual use in driving the display of the dot matrix with the display means, and compression means for an image data, in which

the display area for actual use in driving the display with the display means is reduced in accordance with a predetermined control condition, and the image data compressed by the compression means is displayed in this reduced display area, whereby the display area for use in driving the display can be reduced in accordance with a desired control condition, and the compressed image data can be displayed within this reduced display area, so that there are excellent effects that the electric power necessary for the display can be saved and the display information necessary for the reduced display can be transferred to the user without deficiency.

Next, an another example, a personal information device for dealing with the personal information as shown in Fig. 7 is described. This personal information device has two kinds of display modes for the screen display, i.e., the normal mode and the reduction mode, in which in the reduction mode, a characteristic portion of the display in the normal mode is picked up and displayed in a quarter of the normal size (half vertically and half transversally). In this example the display member is a matrix liquid crystal of 320 x 128 dots as shown in Fig. 3.

Fig. 1 is an electrical block diagram of a display controller for explaining another example. The display controller reads the display data from a video RAM, and transfers its data to a display driver, together with the control signal. In addition, it performs the control for the reduction mode in which the display range is less than the normal display in the normal mode, and the transfer frequency of control signal and data is decreased.

In Fig. 1, 1 is a frequency divider and frequency selector constituted of a counter and a selector. This selects whether the input clock itself (e.g., 667KHz) or the clock with its frequency divided by 1/4 (e.g., 167KHz) is to be used as the clock for the liquid crystal display, depending on the frequency select signal set on the register 2. The clock can be selected in accordance with the display mode. In the normal mode which provides a normal display, the input clock is directly used, while in the reduction mode with the area reduced to a quarter of that in the normal mode, the clock having the input clock frequency divided by 1/4 is used. The clock is output to a line counter 3, a total counter 6 and a liquid crystal clock (CP), as thereafter described.

3 is the line counter for counting synchronously with the clock to get the timing at which the load signal (LOAD) is output. 4 is a register for giving the timing set value to the line counter 3 to set the timing at which the load signal is output, and 5 is a load timing controller for generating and outputting the load signal.

The load signal is input into the liquid crystal driver to latch the input data every time data corresponding to one line of the display matrix is passed to the liquid crystal driver. The liquid crystal driver concurrently receives 4 bits (4 dots) of data for each one clock. Therefore, the load signal is set to be output every time the data of one line of 320 bits have been transferred, i.e., once for every 80 clocks, in the normal mode, or the data of one line of 160 bits have been transferred, i.e., once for every 40 clocks, in the reduction mode.

To set the timing for outputting the load signal, the set value of the timing for outputting the load signal is written into the register 4 by the CPU 19 as will be described later. The line counter 3 reads that set value after the count is terminated, and restarts the count from zero. If the value of the line counter 3 reaches the set value that has been read, the line counter 3 outputs a count termination signal to terminate the count. The load signal is generated when the count termination signal is input into the load timing controller 5 and the signal width of the termination signal is adjusted.

6 is the total counter for counting synchronously with the clock to take the timing at which a frame signal (FRAME) is output, and 8 is a frame signal controller for generating and outputting the frame signal.

7 is a register for giving the timing set value to the total counter 6 to set the timing at which the frame signal is output, 9 is a liquid crystal data controller for controlling the liquid crystal based on the image data and the control data, 10 is a VRAM for storing the image data, and 19 is a CPU which controls the personal information device of the example.

The frame signal is a signal input into the liquid crystal driver every time the image data of one frame is passed to the liquid crystal driver. In this example, the display screen is composed of 320x128 dots in the normal mode, or 160x64 dots in the reduction mode, with which the frame signal is generated as one frame.

To set the timing for outputting the frame signal, the timing set value is written into the register by the CPU 19. The total counter 6 reads that set value after the count is terminated, and restarts the count from zero. If the value of the total counter 6 reaches the set value that has been read, the total counter 6 outputs a count termination signal to terminate the count. The count termination signal is input into the frame signal controller 8 and output as the frame signal.

The timing for outputting the frame signal is set in accordance with the display mode. The frame signal is output for every 1024 clocks in the normal mode because the frame is 320x128 dots, or for every 2560 dots in the reduction mode because the frame is 160x64 dots.

Also, the frame signal controller 8 also generates a signal (DF) for reversing the bias polarity of the liquid crystal for each one frame.

On the other hand, the value of the total counter 6 also serves as the address (address B) for accessing the VRAM 10 which stores the image data. The image data stored in the VRAM 10 is read and written through the liquid crystal data controller 9. The liquid crystal data controller 9 accesses the VRAM 10 by selecting the address A which is addressed by the CPU 19 when the CPU 19 reads and writes the content of the VRAM 10, or selecting the address B which is addressed by the total counter 6 when it reads the image data to be sent to the liquid crystal driver. In this

way, the timings for both address A and address B are controlled not to be overlapped with each other.

Also, the image data read from the VRAM 10, which has one word of 8 bits, is output to the liquid crystal driver as the 4-bit data. Therefore, the liquid crystal data controller 9 divides the image data read from the VRAM 10 into upper 4 bits and lower 4 bits, which are sent to the liquid crystal driver synchronously with the clock (CP). Therefore, the least significant bit (LSB) of the address B is used as a select signal as to whether the upper 4 bits or the lower 4 bits is sent to the liquid crystal driver, and the value of the address B logically shifted one bit to the right is used as the address (address B') of the VRAM 10.

The DISP OFF1 signal and the DISP OFF2 signal set in the register 2 together with the frequency select signal are control signals for turning the display of the liquid crystal driver into the off state (constant output voltage) (in Fig. 1, both signals are represented in the negative logic). In the normal mode, the DISP OFF1 signal and the DISP OFF2 signal are both made "H", while in the reduction mode, only the DISP OFF1 signal is made "L". The DISP OFF1 signal is connected to only the driver not used in the reduction mode, as shown in Figs. 4A and 4B.

The timing waveforms of the operation as above described are shown in Figs. 11A and 11B. Fig. 11A shows the timing waveform in the normal mode, and Fig. 11B shows the timing waveform in the reduction mode.

In Fig. 11A, the timing T0 indicates the time when one frame of image data has been transferred and the frame signal is output. The display of a new frame is started from this timing.

The timing T1 is a timing when the first image data of the new frame is passed to the liquid crystal driver. The address B' points to a leading address of image data in the VRAM 10, in which if the leading data of 8 bits for the image data can be obtained, 4 bits of them are transferred to the liquid crystal driver.

At the timing T2, the value of the address B' is not changed from the value at the timing T1, so that the same memory location is accessed. Among one word of 8 bits of the data thus obtained, remaining 4 bits, except for the 4 bits already transferred at the timing T1, are passed to the liquid crystal driver.

At the timing T3, the address B' is incremented to read the next memory location, 4 bits of which are passed to the liquid crystal driver. This is the same operation as at the timing T1 except for the value of the address B'.

The above operation is repeated until 320 bits (40 words) for one line of the display screen are passed to the liquid crystal driver.

At the timing T4, the last 4 bits among one line of data are passed to the driver. The transfer of data to the liquid crystal driver is made at the eightieth time from the start of transfer for one line of data (at the timing T1), with the address B' being 27HEX indicating the fortieth word. The timing T5 is a timing for outputting the load signal. This terminates the transfer of one line of image data to the liquid crystal driver.

With the above operation, the transfer of image data for one line of 320 bits has been terminated. This is repeated for 128 lines of one frame.

The timing T6 is a timing when the transfer of image data for one frame has been terminated, and the frame signal is output. At this time, the display of one frame in the normal mode can be completed.

Fig. 11B is a timing chart for transferring the image data to the liquid crystal driver in the reduction mode. This is the same procedure as that in Fig. 11A, except for the number of bits constituting one line of the frame, and the number of lines constituting one frame.

The timing T7 is a timing when one frame of image data has been transferred and the frame signal is output. This terminates the display of one frame, and the display of a new frame is started from this timing.

The timing T8 is a timing when the first 4 bits of image data for the new frame is passed to the liquid crystal driver. The address B' points to a leading address of image data in the VRAM 10.

Then, as described in Fig. 11A, the image data is transferred to the liquid crystal driver sequentially each for 4 bits, which is repeated until 160 bits for one line of the frame in the reduction mode has been transferred.

The timing T9 is a timing when the last 4 bits among one line data of the frame are passed to the driver. The transfer of data to the liquid crystal driver is made at the fortieth time from the start of transfer of one line data, with the address B' being 13HEX indicating the twentieth word.

As described in Fig. 11A, the transfer of image data to the liquid crystal driver is repeated by incrementing the value of the address B until one line data has been transferred.

At the timing T10, the data transfer for one line of the frame has been terminated, and the load signal is output.

With the above operation, the transfer of image data for one line of 160 bits has been terminated. This is repeated for 64 lines of one frame.

The timing T11 is a timing when the transfer of image data for one frame has been terminated, and the frame signal is output. At this time, the display of one frame in the reduction mode can be terminated.

By repeating the above procedure, the display in the normal or reduction mode can be made.

Fig. 3 shows the liquid crystal driver circuit. 11 and 12 are command drivers (e.g., MSM5298 made by Oki Electric Industry Co.), and 13, 14, 15 and 16 are segment drivers (e.g., MSM5299 made by Oki Electric Industry Co.). In the normal mode, all the drivers are used, while in the reduction mode, the drivers 11, 13, 14 are used.

Therefore, the signal DISP OFF2 is connected to each of the drivers 11, 13, 14, and the signal DISP OFF1 is

connected to each of the drivers 12, 15, 16 in which if the signal DISP OFF1 signal is "L", the display will disappear except for a left upper quarter portion of the screen. 17 is a liquid crystal panel having a matrix constitution of 320x128 dots. An electronic device of this example is intended to deal with the personal information, in which there are provided the main functions of the universal clock, note screen, address and scheduler. Figs. 12-1A, 12-1B, 12-2A, 12-2B, 12-3A, 12-3B, 12-4A, 12-4B, 12-5A and 12-5B show the examples of representing the above-mentioned functions except for the note screen.

Figs. 12-1A and 12-1B exemplifies the universal clock, Figs. 12-2A and 12-2B the address (cover), Figs. 12-3A and 12-3B the address (telephone list), Figs. 12-4A and 12-4B the scheduler (calendar), and Figs. 12-5A and 12-5B the scheduler (schedule for one day), in which (A) of each view represents the display in the normal mode, while (B) represents the display in the reduction mode, corresponding to (A). In the functions of the universal clock, address and scheduler, the information is written in the screen of fixed form, in which a portion to be picked up for the reduction mode can be predetermined as follows.

The universal clock allows the representation for the Japanese standard time, and the current day and time at the city on the world map by pointing to that city on the world map represented thereon. Thus, the Japanese standard time which is the most important information is displayed on the left upper quarter portion of the screen, as shown in Fig. 12-1B.

The address is to manage the addresses of persons or companies which can be entered in the order of the kana syllabary such as as (ア－オ), (カ－コ) or in a free field which is not in the order of the kana syllabary. Fig. 12-2A which represents the address corresponds to the address index, with which the address in the ア column can be retrieved by pointing to (ア－オ). Thus, a title for the address function and an indication for the kana syllabary index are displayed as the most characteristic portion in the quarter portion of the screen, as shown in Fig. 12-2B.

Fig. 12-3A shows the telephone list for the ヤ column, the leading name of the ア column and its telephone number are displayed in the quarter portion of the screen as shown in Fig. 12-3B.

The scheduler is to manage the schedule of a person, in which the calendar screen is displayed in the normal mode as shown in Fig. 12-4A, while the year, month and day, and the day of week for today are displayed on the quarter portion of the screen as shown in Fig. 12-4B.

In the scheduler (schedule for one day) as shown in Fig. 12-5A are entered the start and end times for the schedule and its requirement. Among them, the date and two schedules with the start time and the requirement (up to six characters), are displayed on the quarter portion of the screen as shown in Fig. 12-5B.

As above, each function of the universal clock, address and scheduler is displayed in a predefined form on the left upper quarter portion of the screen, in the reduction mode.

Figs. 13-1A, 13-1B and Figs. 13-2A, 13-2B show the examples of the note screen in which the character, calculation and drawing can be made freely in the screen, in the normal mode and the reduction mode.

The note screen is a function of permitting the characters, numerical expressions and drawings to be freely written on the blank note. Therefore, the characteristic portion of the display is different for each page of the note, depending on the content to be written. Thus, as shown in Figs. 13-1A and 13-2A, the number of image dots constituting a displayed image is counted for each line of dots, and the lines having maximum number are found in the longitudinal (Y-axis) direction and in the transverse (X-axis) direction, respectively. Around an intersection of dot lines in the longitudinal and transversal directions, a quarter of the display in the normal mode is picked up as the most characteristic portion, and moved to a left upper corner of the screen for the display in the reduction mode as shown in Figs. 13-1B and 13-2B.

Fig. 13-2B can be obtained by moving a normal display image as shown in Fig. 13-1A left upward by the amount of a quarter screen, which is halved longitudinally and transversally, with an intersection (X_{max}, Y_{max}) as the center, with X_{max} being the line having the greatest number of image dots in the longitudinal direction and Y_{max} being the line having the greatest number of image dots in the transverse direction. In the figure, a frame line 34, a page number 35, a lowercase character switch 36 and a dog ear 37 for turning the page are not processed to count the image dot because they are not images drawn by the operator.

As the example of Fig. 13-2A, the frame of the quarter screen may extend out of the screen in the normal mode if the quarter screen is picked up with the center (X_{max}, Y_{max}) of the quarter screen being located toward the end portion. In this case, the pick-up center is moved to (X_{cen}, Y_{max}) in Fig. 13-2A to contain all the quarter frame in the screen, and the quarter frame is set anew. The screen of the reduction mode thus created is shown in Fig. 13-2B.

A flowchart for the procedure of switching the note screen from the normal mode to the reduction mode, which is performed by the CPU 19 as above described, is shown in Fig. 14.

The transfer from the normal mode to the reduction mode takes place in either of the case in which there is no input beyond a fixed time, or there is an instruction from the operator. When switched to the reduction mode, it is first determined which function is currently used among the universal clock, address, scheduler and note screen, and then the screen is changed to each form screen, as shown in Figs. 4A and 4B, except for the note screen. In the note screen, the processing is performed in accordance with the flowchart as shown in Fig. 14.

At step S1, the X-coordinate of row having maximum number of image dots is found by counting the number of

image dots in a longitudinal (Y-axis) direction for all rows. At step S2, the Y-coordinate of line having maximum number of image dots is found by counting the number of image dots in a transverse (X-axis) direction for all lines. From that coordinate as above obtained, the intersection coordinate is obtained at step S3. At step S4, it is determined whether a quarter of the normal screen picked up around that coordinate can be contained within the screen. If it is not contained, the center coordinate is moved so that the quarter frame can be contained within the screen, at step S5.

At step S6, the image data within the quarter frame determined at steps S3 and S5 among the image data stored in the VRAM 10 is once saved into the buffer. At step S7, the VRAM 10 is cleared, and at step S8, the image data saved in the buffer is rewritten into the VRAM 10 so as to be displayed on the left upper quarter portion of the display screen.

At step S9, the display control is set to the reduction mode by setting an appropriate value to the register 2 of Fig. 1.

Note that when there is any input again, or when there is an instruction from the operator, the mode is returned from the reduction mode of quarter screen to the normal mode of full screen.

In the example, the center of the reduced screen was set to the intersection between the line and the row having the greatest density of image dots, but it is also possible to determine the most characteristic screen (having the largest amount of data) by obtaining the maximum value in the extended region such as the addition of five or ten lines, rather than one line or row.

Finally, an external view of a personal information device having a display unit of this example is shown in Fig. 7, and an entire electrical block diagram is shown in Fig. 8.

As shown in Fig. 7, the personal information device of this example is one of inputting a character command on an input/output plane 31 in a combination of a transparent digitizer and a liquid crystal panel, with the handwriting by the use of an input pen 30, and displaying a pen locus, a result of character recognition, and a result of application.

In Fig. 8, VRAM 10 and a liquid crystal panel 17 are the same as those of Fig. 3. 18 is a unit consisting of a liquid crystal data controller (including peripheral circuits as shown in Fig. 1) and a liquid crystal driver, 19 is a 16-bit CPU for controlling this electronic device, 20 is a ROM (Read Only Memory) for storing a procedure as shown in Fig. 14, application programs, OS and dictionary data, 21 is a RAM (Random Access Memory) used for a RAM disk for storage of user data or a work area, 22 is an interface for an IC card, 23 is a serial interface such as RS232C, and 24 is a centronics interface for output to the printer, 25 is a digitizer with the resistive film method, in which two sheets of glass (or one sheet of PET and the other of glass) with a resistive film deposited are opposed and the voltage at the time when two sheets of resistive film are contacted with the pressure of a pen is converted into a coordinate at which the pressure is exerted. 26 is a digitizer driver for obtaining the XY coordinates from an output signal of the digitizer, 27 is an A/D converter for converting the digitizer voltage into a digital value, and 28 is a power source unit including a DC-DC converter.

The display member was described using a simple matrix dot liquid crystal, but an active matrix liquid crystal such as TFT, simple or active matrix EL, or a plasma display can be used likewise in this example.

[Another example]

In the previous example, when the reduction mode is entered because there is no input for a predetermined period or by a user instruction, the screen which appears has been edited with a predefined procedure of the electronic device.

In this example, the note screen allows the selection of an image which the user himself desires to leave most. That is, when the reduction mode is desired, the "reduced screen mode" is selected by opening the menu and pointing to it with the pen 30, and further the "area specification" is selected from a sub menu. Then if any point on the note screen is pointed to, the frame of quarter screen around a pointing spot is displayed superimposed on the screen. Then if the pen is moved while pressing thereon, the frame is moved along with its movement. The spot at which the pen is raised becomes a center coordinate, thereby transferring to the reduction mode. This is illustrated in Figs. 15A and 15B. Fig. 15A shows how the quarter screen is obtained as a frame by pointing to the note screen in the normal mode with the pen. If separating the pen from the screen, specified region is displayed on a left upper portion of the screen in the reduction mode, as shown in Fig. 15B.

Also, with the function having the format display, for example, the address (telephone list), the uppermost data in the telephone list was displayed in the reduction mode, whereas the quarter screen can be constructed to leave specified data on the screen in such a way as to select the "reduced screen mode" by opening the menu, select the "data selection" from the sub menu, and finally point to the telephone data which is desired to leave.

Likewise, the scheduler allows two necessary schedule data to be left on the reduced screen, rather than two schedules initially written. Also, in the universal clock, rather than the Japanese standard time, the standard time of a selected city can be left on the screen in the reduction mode.

As above described, there is an effect that the consumption power can be saved while displaying the information useful for the user at all times, without turning off the power of the device or erasing the display screen completely.

Claims

1. A display means for displaying a dot matrix, comprising

   i) input means (25) for inputting image information,
   ii) storing means (10) for storing image information to be displayed, and
   iii) a display unit (17) for displaying the stored information,

   said display means being **characterized by** further comprising:

   iv) a control means (1 - 9) portion for variably controlling the number of lines or rows for actual use in driving the display of the dot matrix with the display unit,
   v) a control means (1 - 9) portion for reducing the display area for actual use in driving the display with the display unit and displaying the image information reduced by reduction means in this reduced area, and
   vi) a control means (1 - 9) portion for controlling the switching between a normal screen display using the entire display screen and a screen display for reduced image area if a predetermined period of time has elapsed since the last input operation.

2. The display means according to claim 1, characterized in that said control means (1 - 9) is adapted to activate a part of said display unit (17) and to deactivate the remainder thereof.

3. The display means according to any of the claims 1 and 2, characterized by further comprising image edit means, said image edit means being adapted to pick up and re-edit a portion of a normally displayed image, to create the image to be displayed in said reduced image area.

4. The display means according to any of the preceding claims, characterized in that said control means (1 - 9) is adapted to decrease the frequency of a data transfer clock.

5. The display means according to any of the preceding claims, characterized by further comprising a control means (1 - 9) portion for compressing the stored image information, wherein, in operation, the display area for actual use in driving the display with the display means is reduced, and image information compressed by compression means is displayed in this reduced area.

6. The display means according to any of the preceding claims, characterized by further comprising means for performing a smoothing of an image data as well as a compression of image data in said display region at the reduction.

7. The display means according to any of the claims 5 and 6, characterized in that said compressing means is adapted to compress the information by giving weights to a plurality of pixels constituting the information.

8. A method for displaying information, comprising the steps

   i) inputting image information,
   ii) storing the image information to be displayed, and
   iii) displaying the stored information,

   said method being **characterized by** further comprising the steps of

   iv) variably controlling the number of lines or rows for actual use in driving the display of a dot matrix,
   v) reducing the display area for actual use in driving the display and displaying the reduced image information in this reduced area, and
   vi) controlling the switching between a normal screen display using the entire display screen and a screen display for a reduced image area if a predetermined period of time has elapsed since the last input operation.

9. The method according to claim 8, characterized by the step of activating a part of a display unit (17) and by the step of deactivating the remainder thereof, if said screen display for the reduced image area is to be used.

10. The method according to any of the claims 8 and 9, characterized by further comprising the step of picking up and re-editing a portion of a normally displayed image, to create the image to be displayed in said reduced image area.

11. The method according to any of the claims 8 to 10, characterized by the step of decreasing the frequency of a data transfer clock, if said screen display for the reduced image area is to be used.

12. The method according to any of the claims 8 to 11, characterized by further comprising the step of compressing the stored image information, wherein, in operation, the display area for actual use in driving the display is reduced, and compressed image information is displayed in this reduced area.

13. The display means according to any of the claims 8 to 12, characterized by further comprising the step of performing a smoothing of an image data as well as a compression of image data in said display region at the reduction.

14. The method according to any of the claims 12 and 13, characterized in that the compression of the information is performed by giving weights to a plurality of pixels constituting the information.

Patentansprüche

1. Anzeigeeinrichtung zur Anzeige einer Punktmatrix mit

   i) Eingabeeinrichtung (25) zum Eingeben von Bildinformation,
   ii) Speichereinrichtung (10) zum Speichern der anzuzeigenden Bildinformation und
   iii) Anzeigeeinheit (17) zum Anzeigen der gespeicherten Information

   gekennzeichnet dadurch, daß sie weiter enthält:

   iv) Steuerungseinrichtungsteil (1 - 9) zur variablen Steuerung der Anzahl von Zeilen oder Reihen zur wirksamen Verwendung beim Antrieb der Anzeige der Punktmatrix mit der Anzeigeeinheit,
   v) Steuerungeinrichtungsteil (1 - 9) zur Verkleinerung des Anzeigebereichs zur wirksamen Verwendung beim Antrieb der Anzeige mit der Anzeigeeinheit und zur Anzeige der von der Verkleinerungseinrichtung in diesem verkleinerten Bereich angezeigten Bildinformation und
   vi) Steuerungseinrichtungsteil (1 - 9) zur Steuerung des Umschaltens zwischen einer normalen Bildschirmanzeige unter Verwendung des gesamten Anzeigenbildschirms und einer Bildschirmanzeige für den verkleinerten Bildbereich, wenn eine vorher bestimmte Zeitdauer seit dem letzten Eingabevorgang vergangen ist.

2. Anzeigeeinrichtung nach Anspruch 1,
   gekennzeichnet dadurch, daß die Steuerungseinrichtung (1 - 9) in der Lage ist, einen Teil der Anzeigeeinheit 17 zu aktivieren und das von ihr Verbleibende zu deaktivieren.

3. Anzeigeeinrichtung nach Anspruch 1 und 2,
   gekennzeichnet dadurch, daß sie weiter eine Bildausgabeeinrichtung enthält, die in der Lage ist, einen Teil eines normal angezeigten Bildes zur Erzeugung des Bildes, das im verkleinerten Bildbereich angezeigt werden soll, aufzunehmen und wieder auszugeben.

4. Anzeigeeinrichtung nach den vorigen Ansprüchen,
   gekennzeichnet dadurch, daß die Steuerungseinrichtung (1 - 9) in der Lage ist, die Frequenz eines Datenübertragungstaktes zu vermindern.

5. Anzeigeeinrichtung nach den vorigen Ansprüchen,
   gekennzeichnet dadurch, daß sie weiter einen Steuerungseinrichtungsteil (1 - 9) zum Komprimieren der gespeicherten Bildinformation enthält, in dem während des Betriebs der Anzeigebereich zur wirksamen Verwendung beim Antrieb der Anzeige mit der Anzeigeneinrichtung verkleinert wird und von einer Komprimiereinrichtung komprimierte Bildinformation in diesem verkleinerten Bereich angezeigt wird.

6. Anzeigeeinrichtung nach den vorigen Ansprüchen,
   gekennzeichnet dadurch, daß sie weiter eine Einrichtung zur Durchführung sowohl einer Glättung von Bilddaten als auch einer Komprimierung von Bilddaten im Anzeigegebiet bei der Verkleinerung enthält.

7. Anzeigeeinrichtung nach Anspruch 5 und 6,
   gekennzeichnet dadurch, daß die Komprimierungseinheit in der Lage ist, die Information durch Gewichtung einer

Vielzahl von Pixeln, die die Information darstellen, zu komprimieren.

8. Verfahren zum Anzeigen von Information mit den Schritten

i) Eingabe von Bildinformation,
ii) Speicherung der anzuzeigenden Bildinformation und
iii) Anzeige der gespeicherten Information,

gekennzeichnet dadurch, daß das Verfahren weiter folgende Schritte enthält

iv) variable Steuerung der Anzahl der Zeilen oder Reihen zur wirksamen Verwendung beim Antrieb der Anzeige einer Punktmatrix,
v) Verkleinerung des Anzeigebereichs zur wirksamen Verwendung beim Antrieb der Anzeige und Anzeige der verkleinerten Bildinformation in diesem verkleinerten Bereich und
vi) Steuerung des Umschaltens zwischen einer normalen Bildschirmanzeige unter Verwendung des gesamten Anzeigenbildschirms und einer Bildschirmanzeige für den verkleinerten Bildbereich wenn eine vorher bestimmte Zeitdauer seit dem letzten Eingabevorgang vergangen ist.

9. Verfahren nach Anspruch 8,
gekennzeichnet durch den Schritt der Aktivierung eines Teils einer Anzeigeeinheit (17) und den Schritt der Deaktivierung des von ihr Verbleibenden, wenn der Anzeigenbildschirm für den verkleinerten Bildbereich verwendet werden soll.

10. Verfahren nach Anspruch 8 und 9,
gekennzeichnet dadurch, daß es weiter den Schritt der Aufnahme und Wiedergabe eines Teils eines normal angezeigten Bildes zur Erzeugung des Bildes, das im verkleinerten Bildbereich angezeigt werden soll, enthält.

11. Verfahren nach Anspruch 8 bis 10,
gekennzeichnet durch den Schritt der Verminderung der Frequenz eines Datenübertragungstaktes, wenn die Bildschirmanzeige für den verkleinerten Bildbereich verwendet werden soll.

12. Verfahren nach Anspruch 8 bis 11,
gekennzeichnet dadurch, daß es weiter den Schritt der Komprimierung der gespeicherten Bildinformation enthält, bei dem, während des Betriebs, der Anzeigebereich zur wirksamen Verwendung beim Antrieb der Anzeige verkleinert wird und komprimierte Bildinformation in diesem verkleinerten Bereich angezeigt wird.

13. Anzeigeeinrichtung nach Anspruch 8 bis 12,
gekennzeichnet dadurch, daß sie weiter den Schritt der Durchführung sowohl einer Glättung von Bilddaten als auch einer Komprimierung von Bilddaten im Anzeigegebiet bei der Verkleinerung enthält.

14. Verfahren nach Anspruch 12 und 13,
gekennzeichnet dadurch, daß die Komprimierung der Information durch Gewichtung einer Vielzahl von Pixeln, die die Information darstellen, durchgeführt wird.

Revendications

1. Moyens d'affichage pour l'affichage d'une matrice de points comprenant

i) des moyens d'entrée (25) pour introduire de l'information d'image,
ii) des moyens de mémorisation (10) pour mémoriser de l'information d'image devant être affichée; et
iii) une unité d'affichage (17) pour afficher l'information mémorisée,

lesdits moyens d'affichage étant caractérisés en ce qu'ils comprennent en outre :

iv) une partie formant moyens de commande (1-9) pour commander de façon variable le nombre de lignes ou de rangées destinées à être utilisées effectivement pour la commande de l'affichage de la matrice de points avec l'unité d'affichage,

v) une partie formant moyens de commande (1-9) pour réduire la zone d'affichage pour une utilisation effective lors de la commande de l'affichage avec l'unité d'affichage et afficher l'information d'image, réduite par les moyens de réduction dans cette zone réduite, et
vi) une partie formant moyens de commande (1-9) pour commander la commutation d'un affichage d'écran normal utilisant l'ensemble de l'écran d'affichage et un affichage d'écran pour une zone d'image réduite si un intervalle de temps prédéterminé s'est écoulé depuis la dernière opération d'entrée.

2. Moyens d'affichage selon la revendication 1, caractérisés en ce que lesdits moyens de commande (1-9) sont adaptés pour activer une partie de ladite unité d'affichage (17) et désactiver le reste de cette unité.

3. Moyens d'affichage selon l'une quelconque des revendications 1 et 2, caractérisés en ce qu'ils comportent en outre des moyens d'édition d'image, lesdits moyens d'édition d'images étant adaptés pour détecter et rééditer une partie d'une image affichée normalement, pour créer l'image devant être affichée dans ladite zone d'image réduite.

4. Moyens d'affichage selon l'une quelconque des revendications précédentes, caractérisés en ce que lesdits moyens de commande (1-9) sont adaptés pour réduire la fréquence d'un signal d'horloge de transfert de données.

5. Moyens d'affichage selon l'une quelconque des revendications précédentes, caractérisés en ce qu'ils comportent en outre une partie formant moyens de commande (1-9) pour comprimer l'information d'image mémorisée, auquel cas, en fonctionnement, la zone d'affichage pour l'utilisation effective lors de la commande de l'affichage avec les moyens d'affichage est réduite, et l'information d'image comprimée par des moyens de compression est affichée dans cette zone réduite.

6. Moyens d'affichage selon l'une quelconque des revendications précédentes, caractérisés en ce qu'ils comportent en outre des moyens pour effectuer un lissage de données d'image ainsi qu'une compression de données d'image dans ladite région d'affichage lors de la réduction.

7. Moyens d'affichage selon l'une quelconque des revendications 5 et 6, caractérisés en ce que lesdits moyens de compression sont adaptés pour comprimer l'information en appliquant des poids à une pluralité de pixels constituant l'information.

8. Procédé d'affichage d'une information, comprenant les étapes consistant à :

i) introduire de l'information d'image,
ii) mémoriser l'information d'image devant être affichée, et
iii) afficher l'information mémorisée,

ledit procédé étant caractérisé en ce qu'il comprend en outre les étapes consistant à

iv) commander d'une manière variable le nombre de lignes ou de rangées pour une utilisation effective pour la commande de l'affichage d'une matrice de points,
v) réduire la zone d'affichage pour une utilisation effective pour la commande de l'affichage et afficher l'information d'image réduite dans cette zone réduite, et
vi) commander la commutation entre un affichage d'écran normal utilisant l'ensemble de l'écran d'affichage, et un affichage d'écran pour une zone d'image réduite, si un intervalle de temps prédéterminé s'est écoulé depuis la dernière opération d'entrée.

9. Procédé selon la revendication 8, caractérisé par l'étape consistant à activer une partie de l'unité d'affichage (17) et par l'étape consistant à désactiver le reste de cette unité, si ledit affichage d'écran pour la zone d'image réduite doit être utilisé.

10. Procédé selon l'une quelconque des revendications 8 et 9, caractérisé en ce qu'il comprend en outre l'étape consistant à détecter et rééditer une partie d'une image affichée normalement, pour créer l'image devant être affichée dans ladite zone d'image réduite.

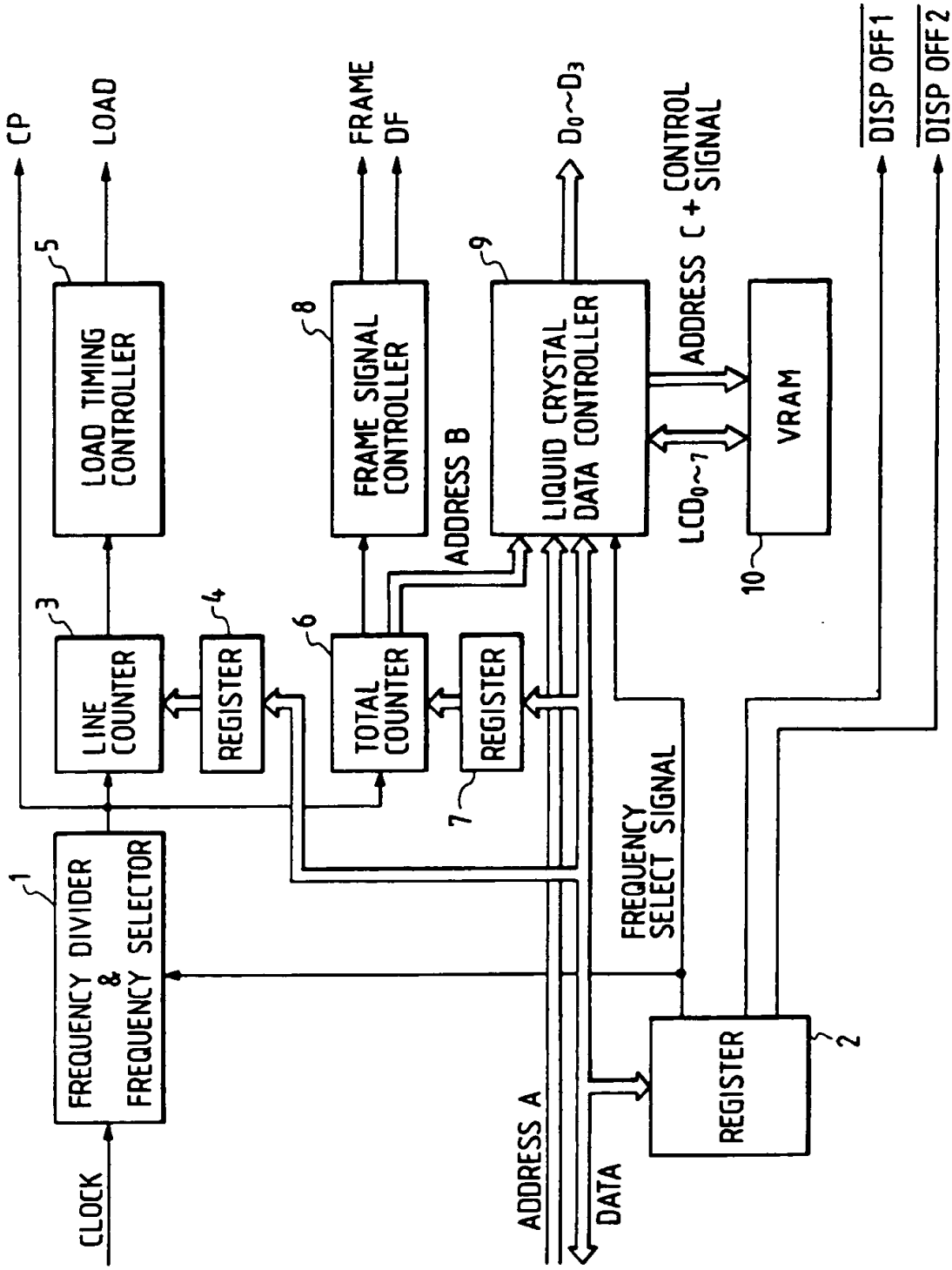
11. Procédé selon l'une quelconque des revendications 8 à 10, caractérisé par l'étape consistant à réduire la fréquence d'un signal d'horloge de transfert de données, si ledit affichage de l'écran pour la zone d'image réduite doit être utilisé.

12. Procédé selon l'une quelconque des revendications 8 à 11, caractérisé en ce qu'il comporte en outre l'étape consistant à comprimer l'information d'image mémorisée, auquel cas, en fonctionnement, la zone d'image pour une utilisation effective pour la commande de l'affichage est réduite, et une information d'image comprimée est affichée dans cette zone réduite.

13. Moyens d'affichage selon l'une quelconque des revendications 8 à 12, caractérisés en ce qu'ils comprennent en outre l'étape consistant à exécuter un lissage des données d'image ainsi qu'une compression des données d'image dans ladite zone d'affichage lors de la réduction.

14. Procédé selon l'une quelconque des revendications 12 et 13, caractérisé en ce que la compression de l'information est exécutée par l'application de poids à une pluralité de pixels constituant l'information.

FIG. 1


CP
LOAD
FRAME DF
D0~D3
DISP OFF1
DISP OFF2
LOAD TIMING CONTROLLER
FRAME SIGNAL CONTROLLER
LIQUID CRYSTAL DATA CONTROLLER
ADDRESS C + CONTROL SIGNAL
VRAM
LCD0~7
ADDRESS B
LINE COUNTER
REGISTER
TOTAL COUNTER
REGISTER
FREQUENCY DIVIDER & FREQUENCY SELECTOR
FREQUENCY SELECT SIGNAL
CLOCK
ADDRESS A
DATA
REGISTER
1
2
3
4
5
6
7
8
9
10

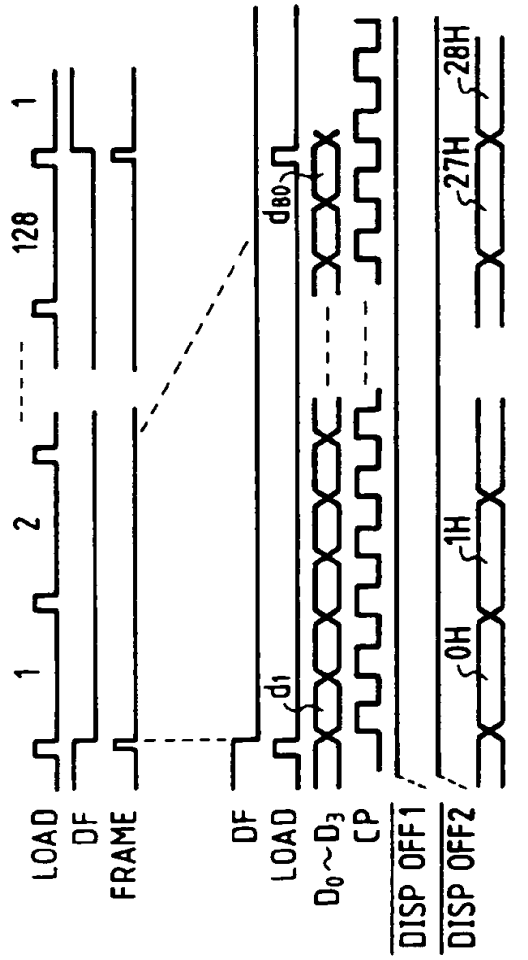

LOAD
DF
FRAME
1
2
128
1
DF
LOAD
D0~D3
CP
d1
d80
DISP OFF1
DISP OFF2
0H
1H
27H
28H

FIG. 2A

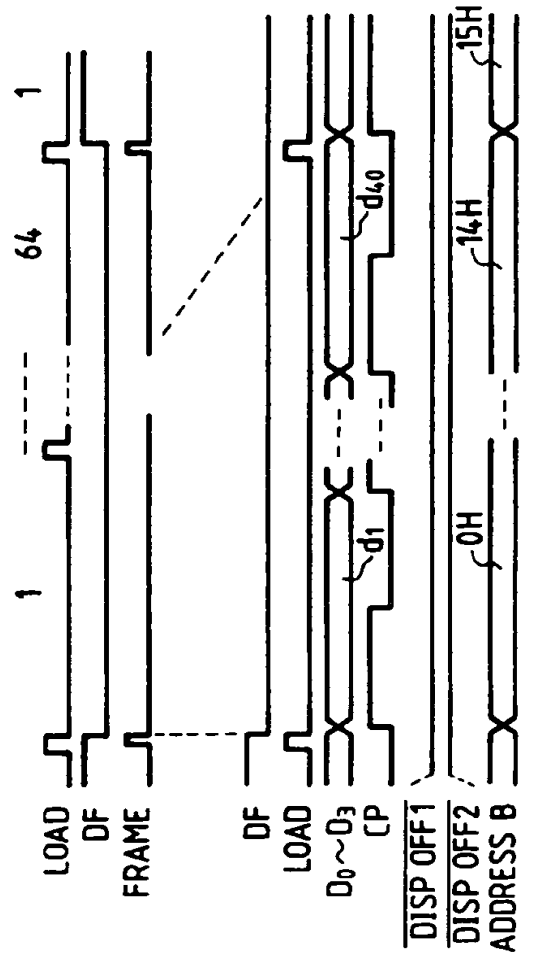

LOAD
DF
FRAME
1
1
64
1
DF
LOAD
D0~D3
CP
d1
d40
DISP OFF1
DISP OFF2
ADDRESS B
0H
14H
15H

FIG. 2B

FIG. 3

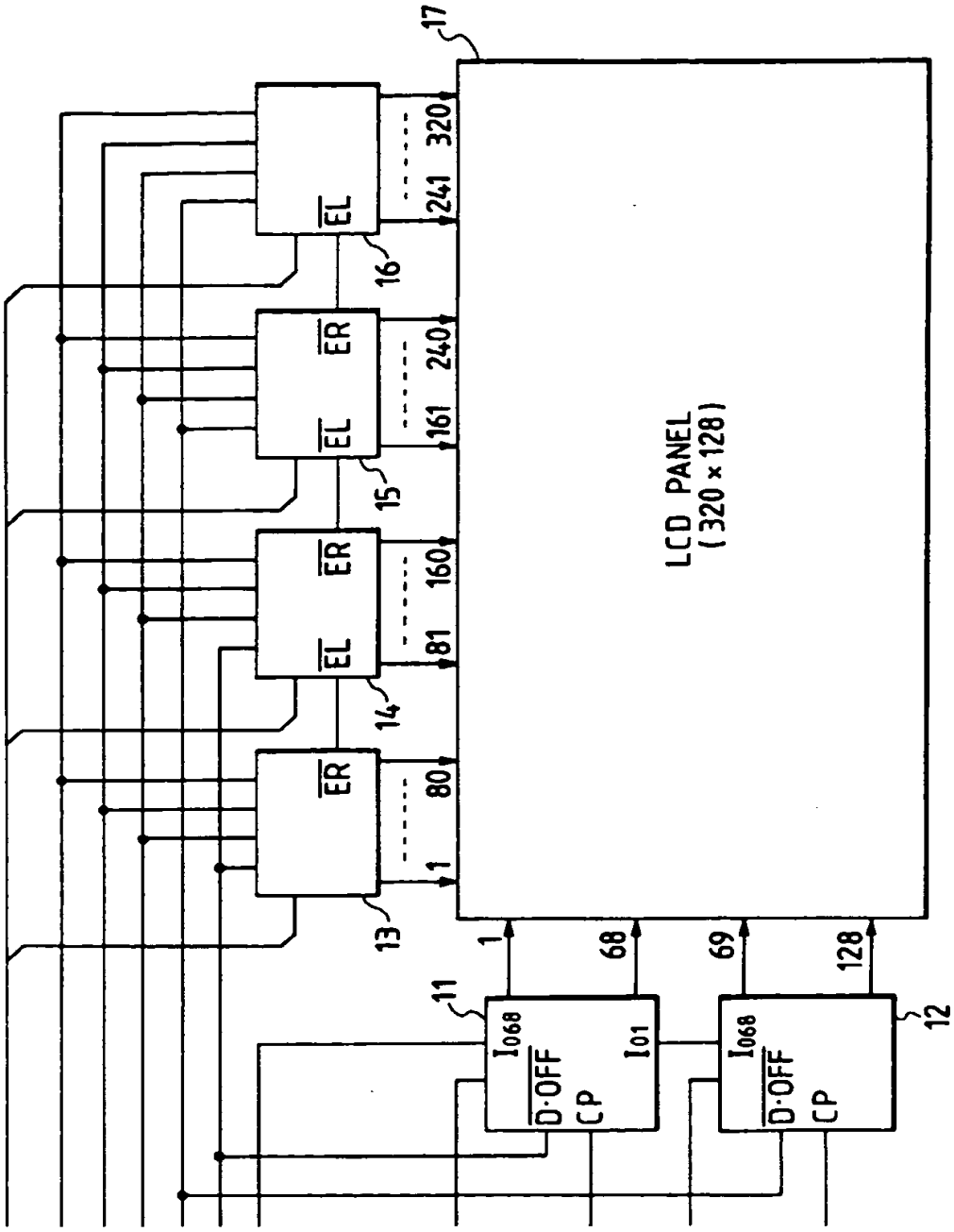

17
LCD PANEL
(320 × 128)
320
241
240
161
160
81
80
1
EL
ER
16
15
14
13
1
68
69
128
11
12
I068
I01
D·OFF
CP

FIG. 4A

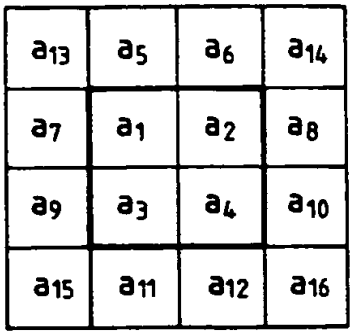


FIG. 4B

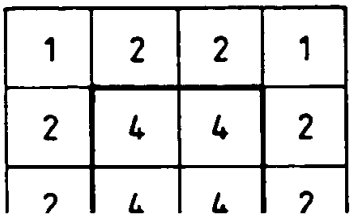


FIG. 5

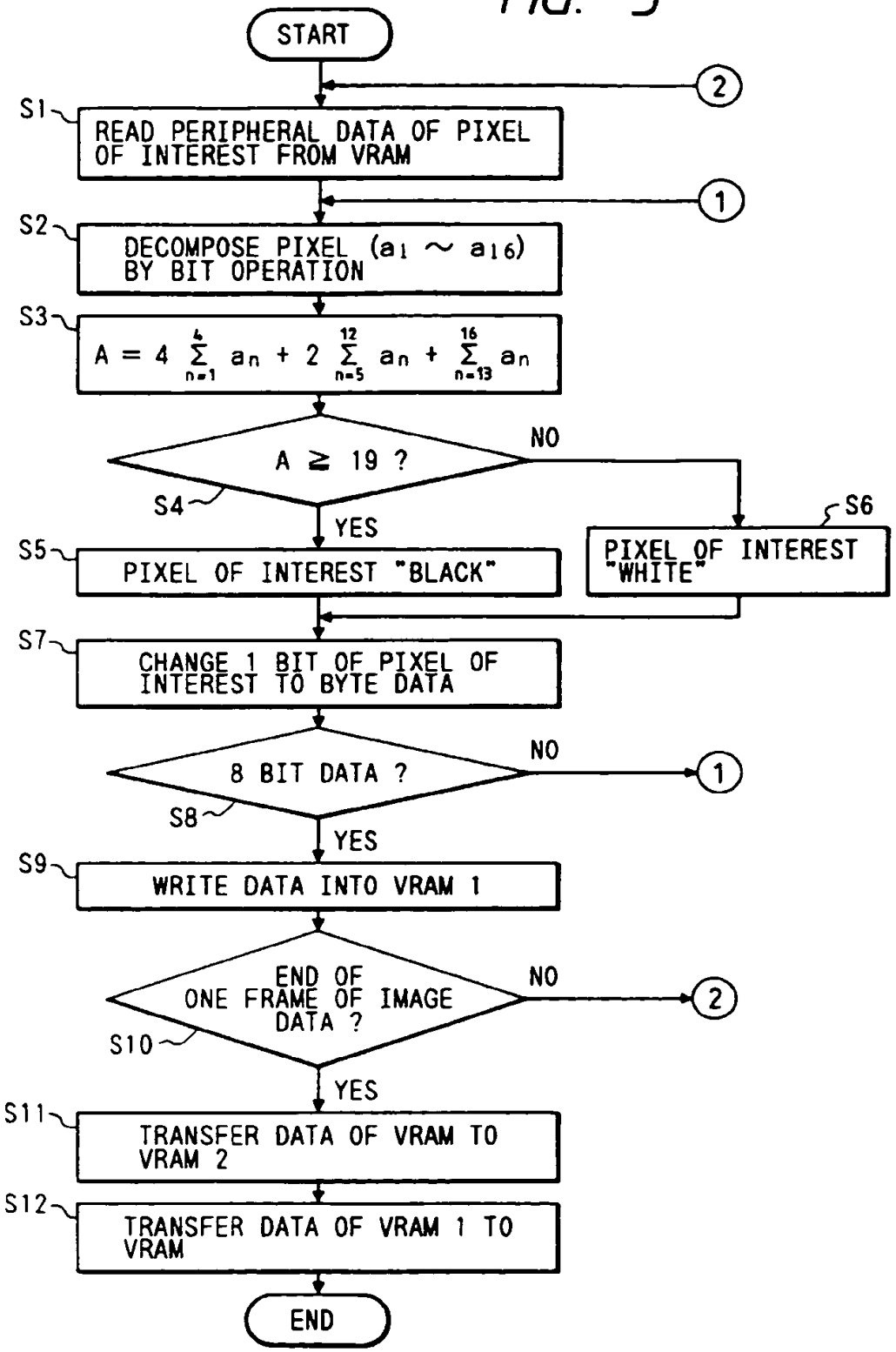

START
2
S1
READ PERIPHERAL DATA OF PIXEL OF INTEREST FROM VRAM
1
S2
DECOMPOSE PIXEL ($a_1 \sim a_{16}$) BY BIT OPERATION
S3
$A = 4 \sum_{n=1}^{4} a_n + 2 \sum_{n=5}^{12} a_n + \sum_{n=13}^{16} a_n$
A ≧ 19 ?
NO
S4
YES
S6
PIXEL OF INTEREST "WHITE"
S5
PIXEL OF INTEREST "BLACK"
S7
CHANGE 1 BIT OF PIXEL OF INTEREST TO BYTE DATA
8 BIT DATA ?
NO
1
S8
YES
S9
WRITE DATA INTO VRAM 1
END OF ONE FRAME OF IMAGE DATA ?
NO
2
S10
YES
S11
TRANSFER DATA OF VRAM TO VRAM 2
S12
TRANSFER DATA OF VRAM 1 TO VRAM
END

FIG. 6A

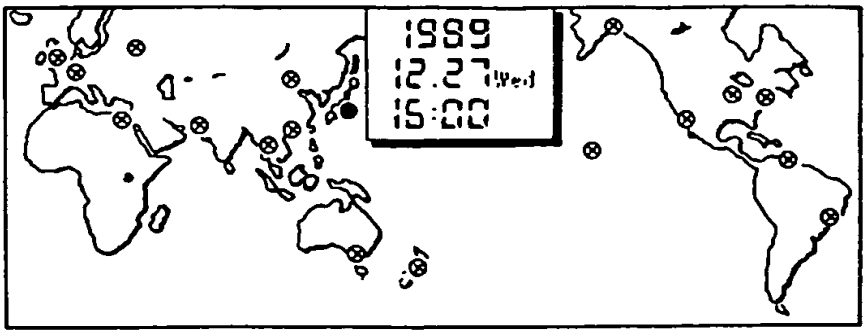


FIG. 6B

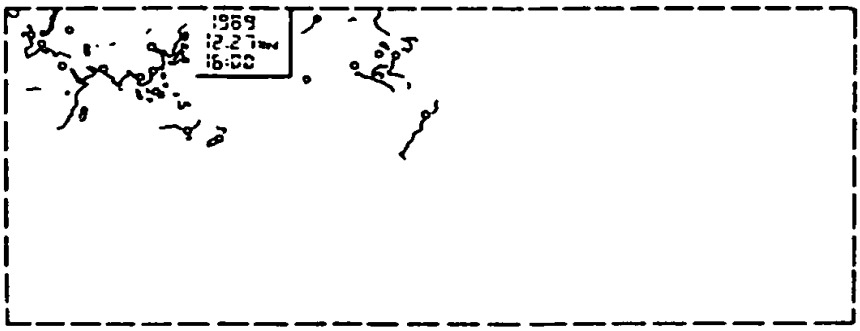


FIG. 6C

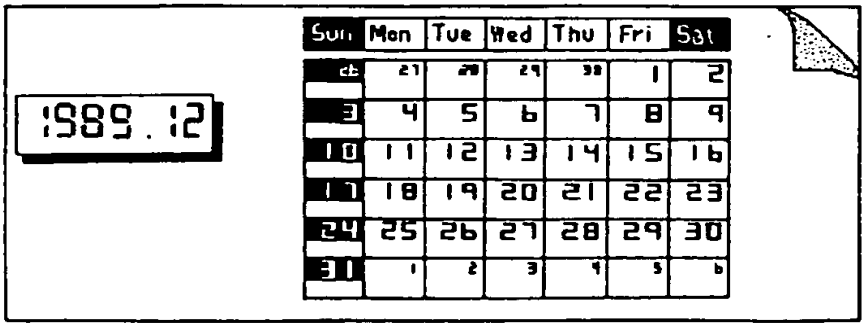


FIG. 6D

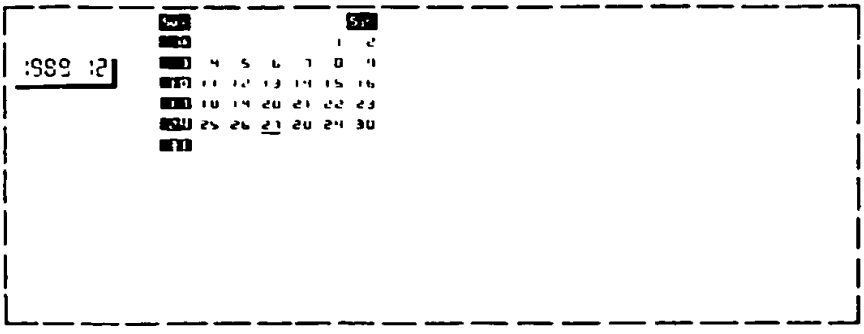


FIG. 7

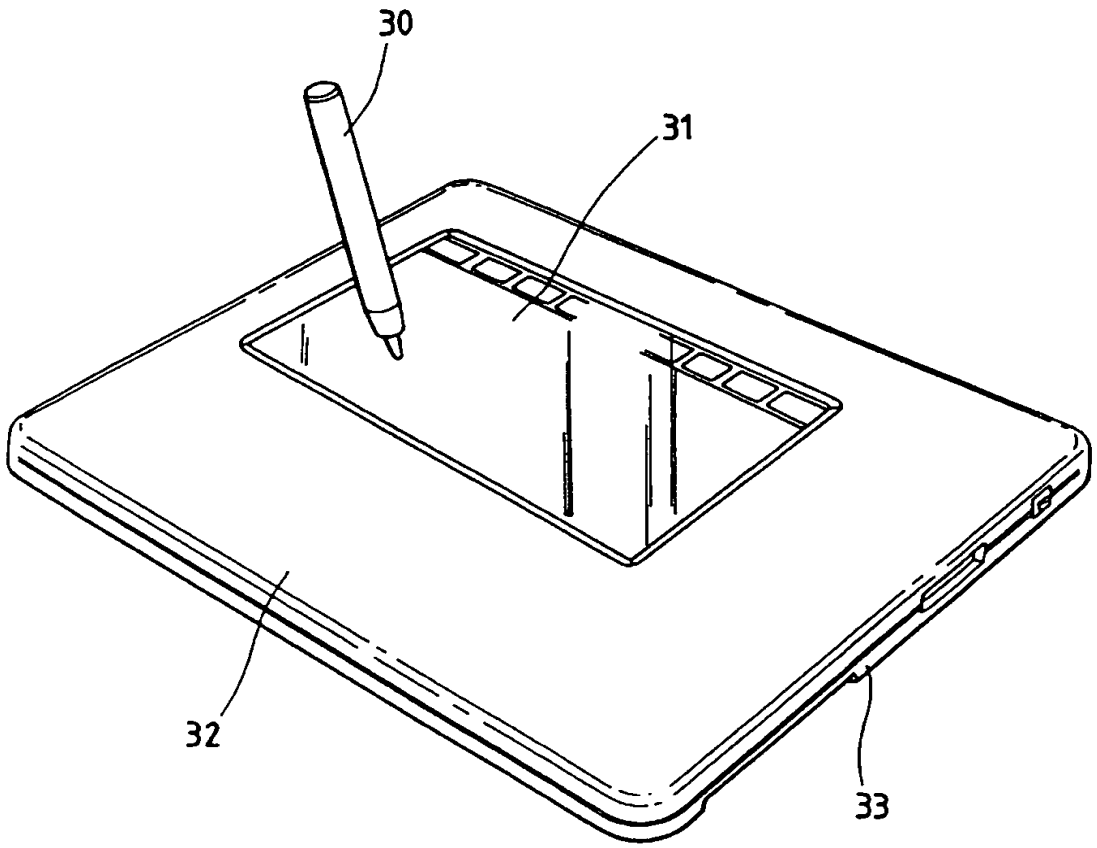


FIG. 8

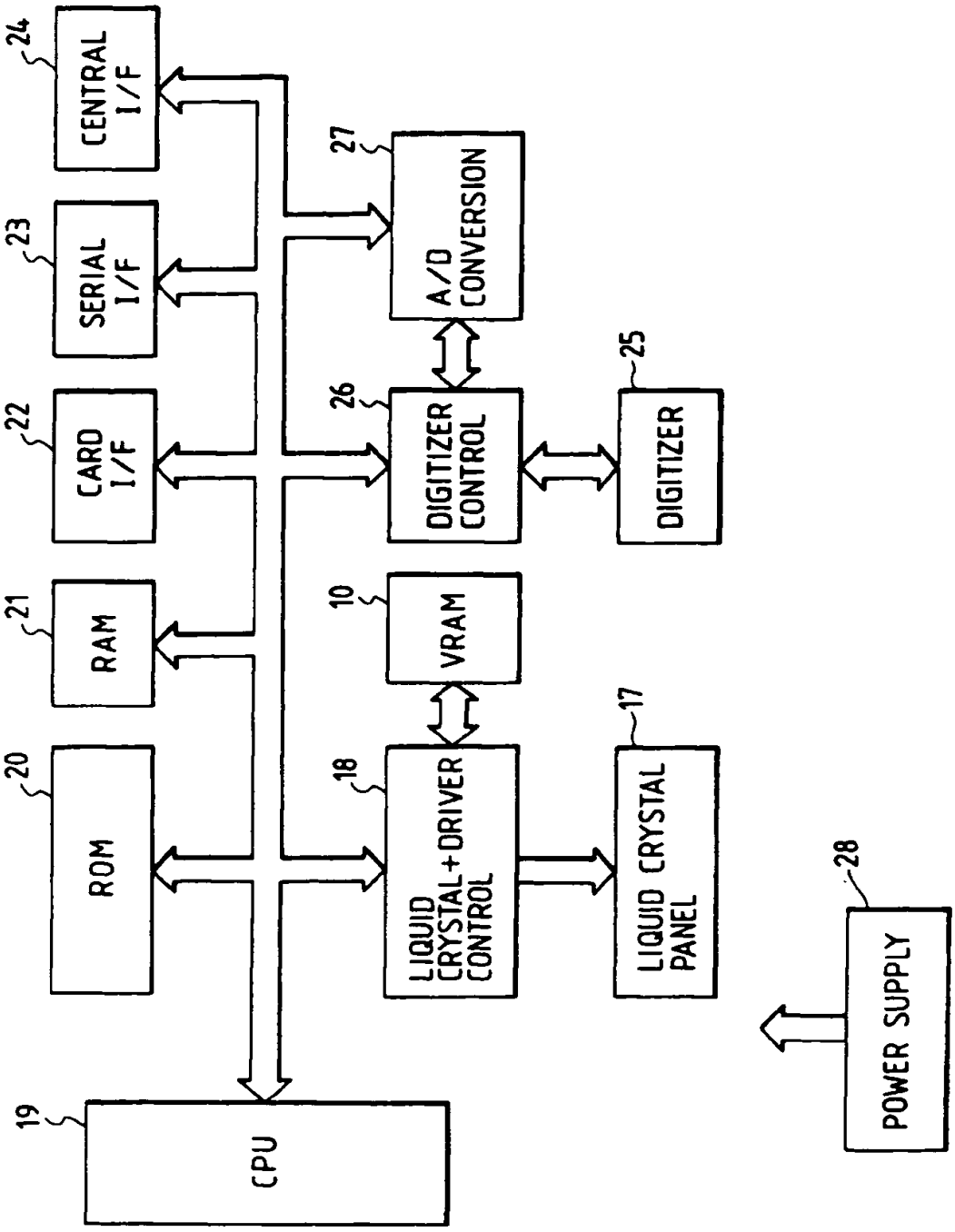

24
CENTRAL I/F
23
SERIAL I/F
22
CARD I/F
21
RAM
20
ROM
19
CPU
27
A/D CONVERSION
26
DIGITIZER CONTROL
25
DIGITIZER
10
VRAM
18
LIQUID CRYSTAL+DRIVER CONTROL
17
LIQUID CRYSTAL PANEL
28
POWER SUPPLY

FIG. 9

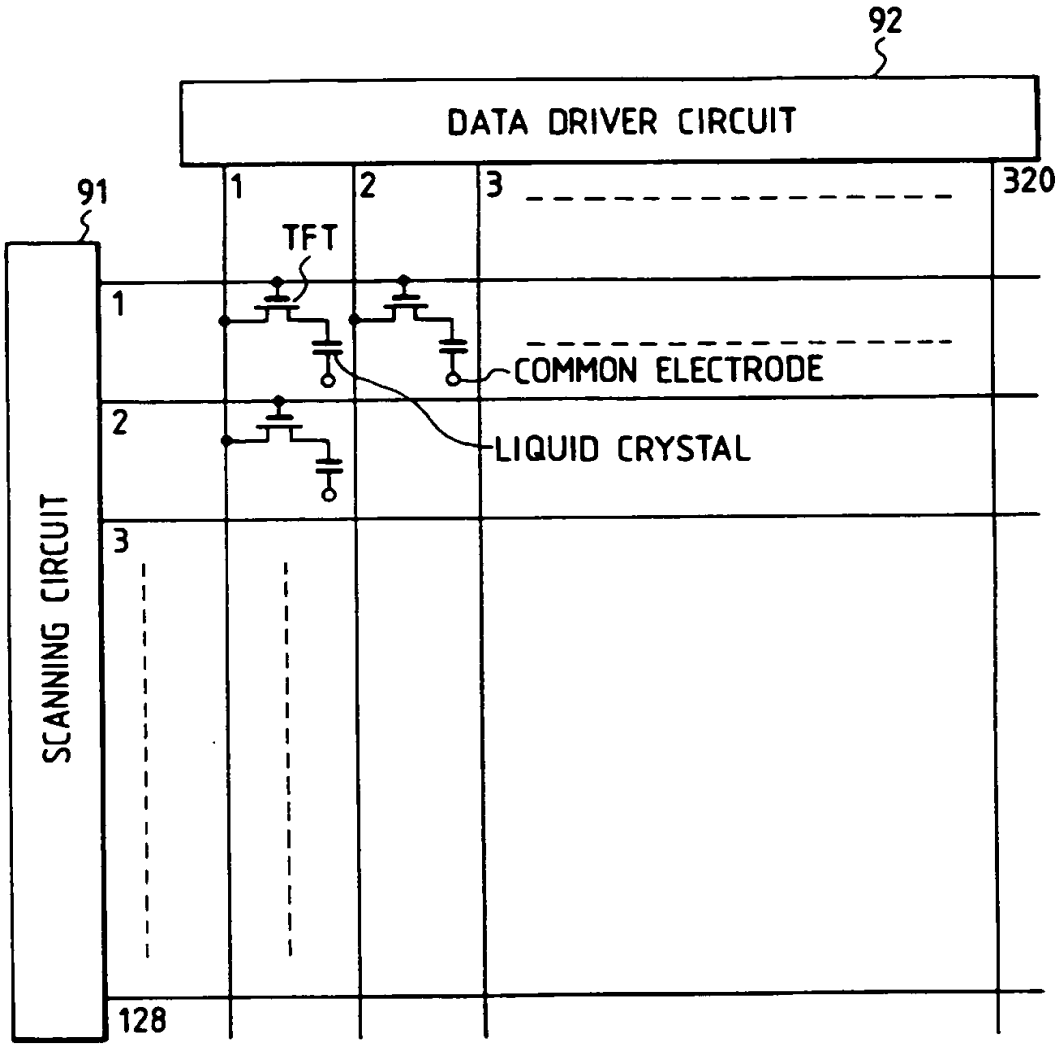

92
DATA DRIVER CIRCUIT
91
1
2
3
320
TFT
1
COMMON ELECTRODE
2
LIQUID CRYSTAL
3
SCANNING CIRCUIT
128

FIG. 10

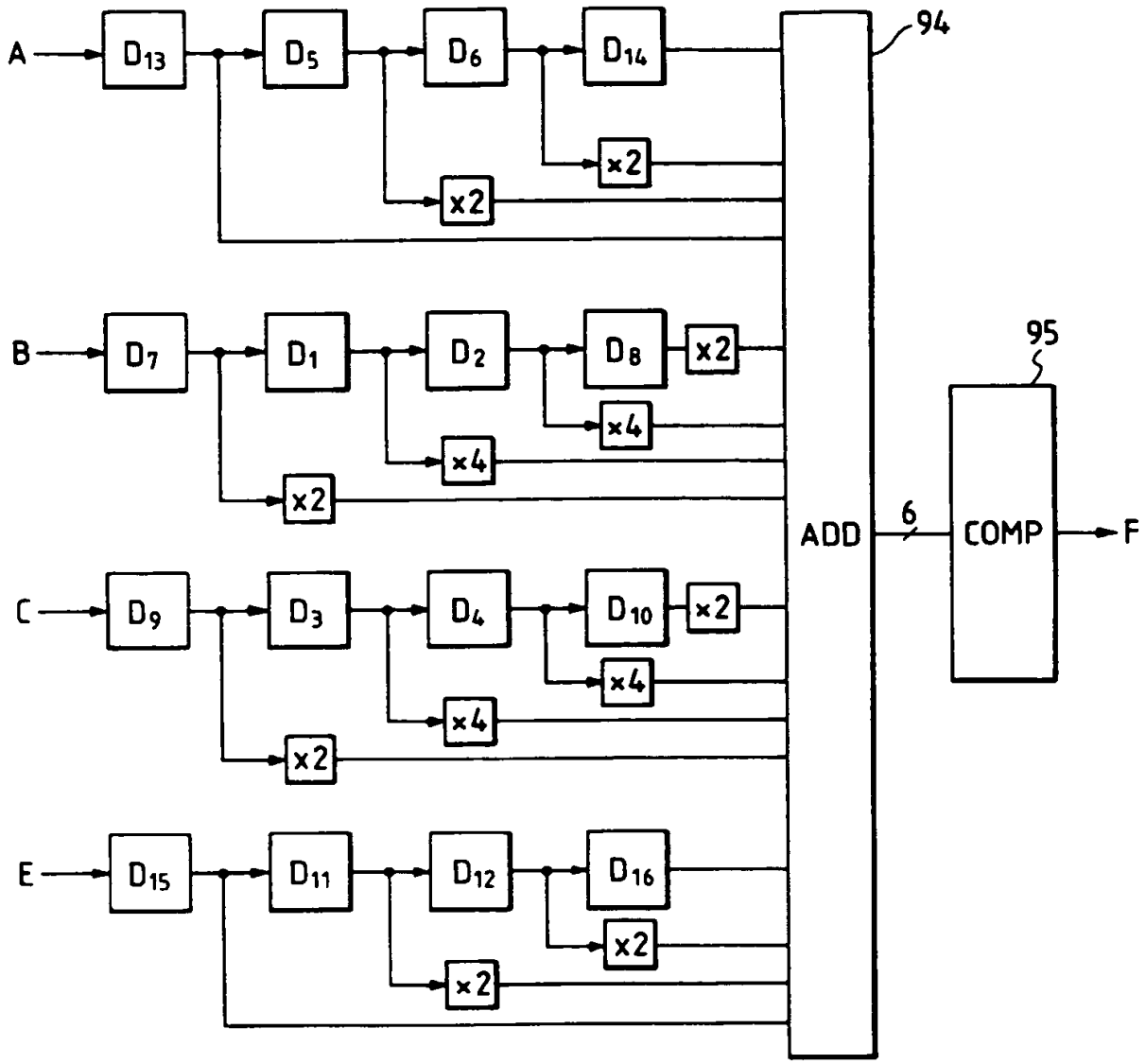

A
B
C
E
D13
D5
D6
D14
D7
D1
D2
D8
D9
D3
D4
D10
D15
D11
D12
D16
x2
x4
94
95
ADD
6
COMP
F

FIG. 11A

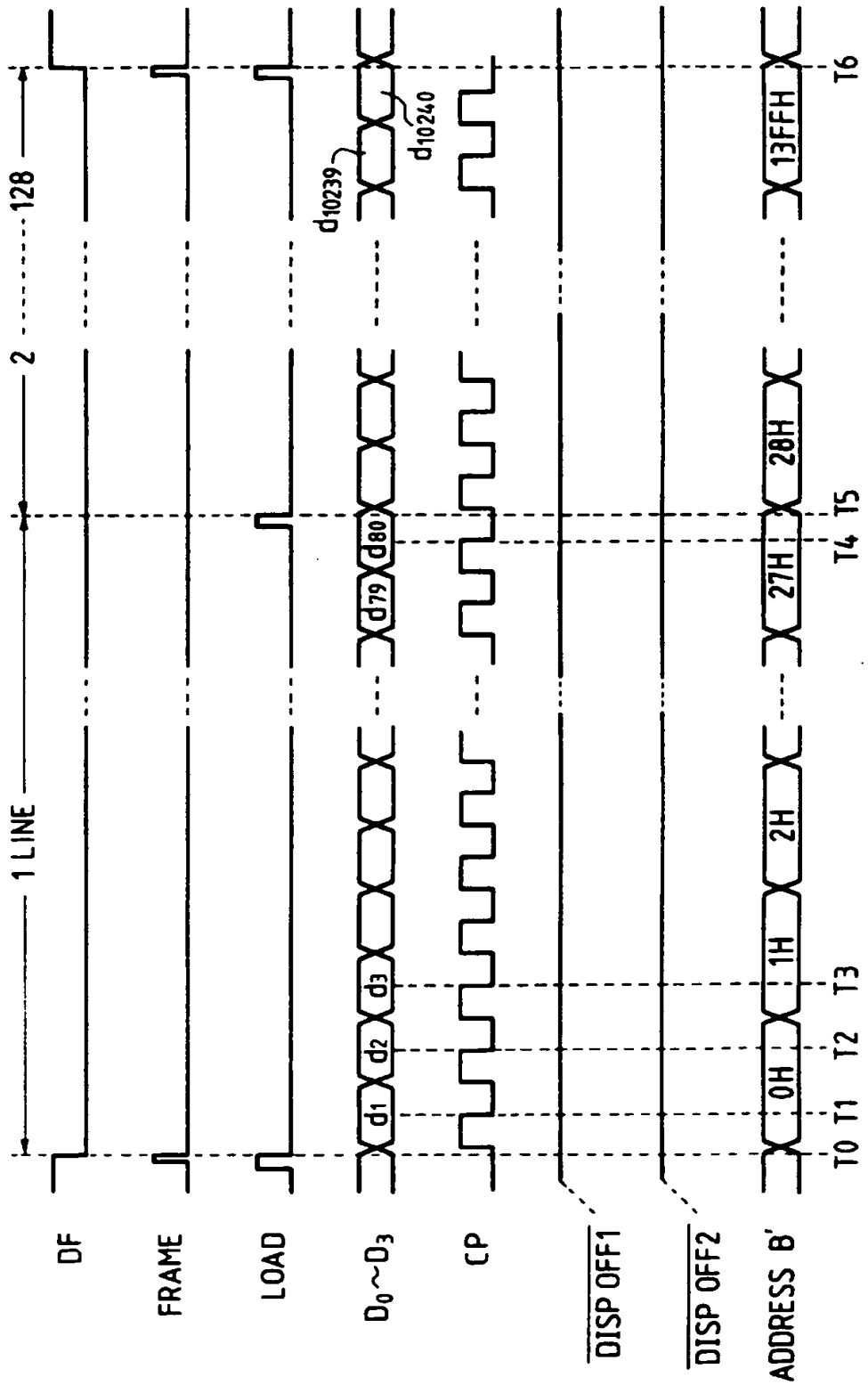

1 LINE
2
128
DF
FRAME
LOAD
D0~D3
CP
DISP OFF1
DISP OFF2
ADDRESS B'
d1
d2
d3
d79
d80
d10239
d10240
0H
1H
2H
27H
28H
13FFH
T0 T1
T2
T3
T4 T5
T6

FIG. 11B

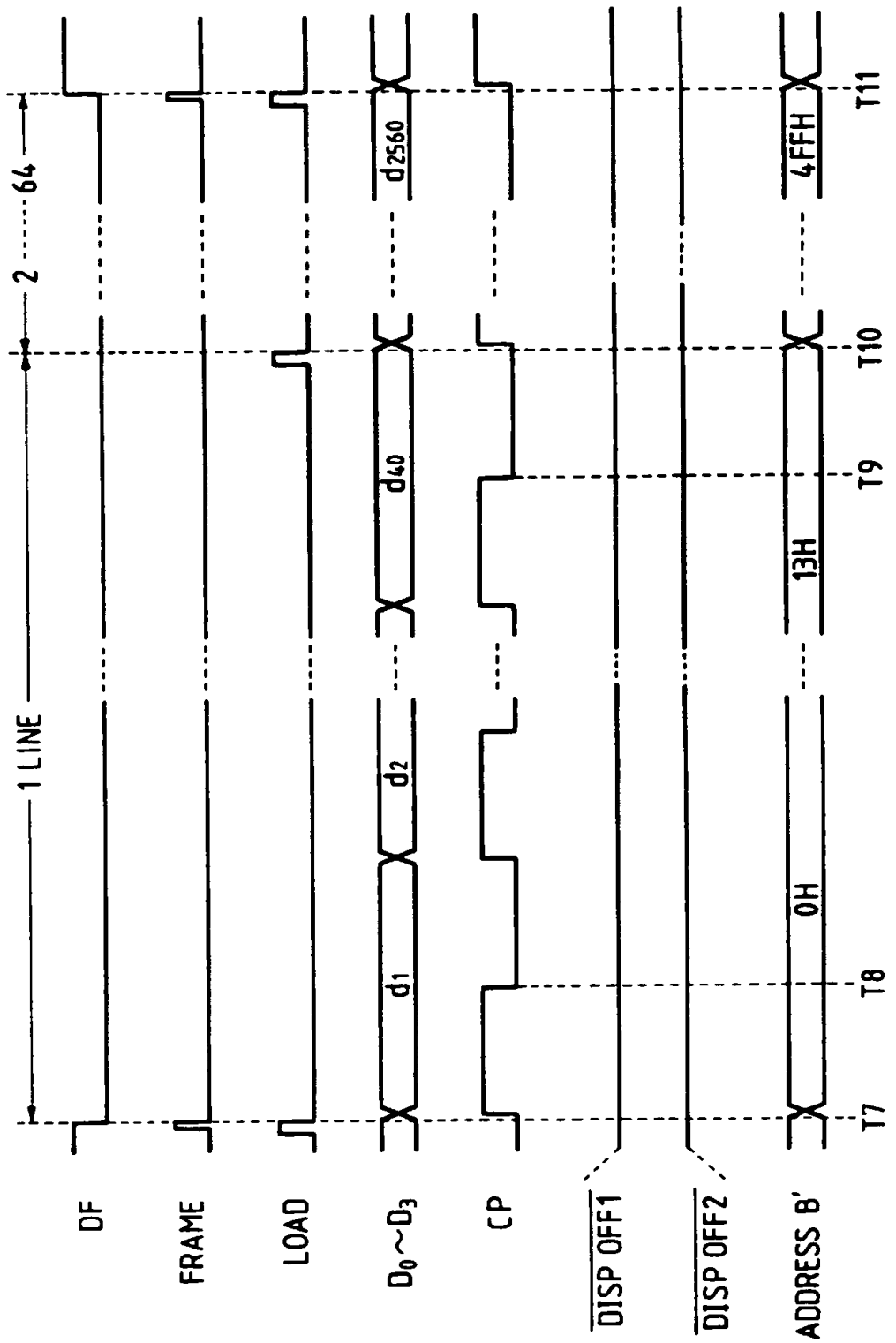

1 LINE
2
64
DF
FRAME
LOAD
$D_0 \sim D_3$
CP
DISP OFF1
DISP OFF2
ADDRESS B'
d1
d2
d40
d2560
0H
13H
4FFH
T7
T8
T9
T10
T11

FIG. 12-1A

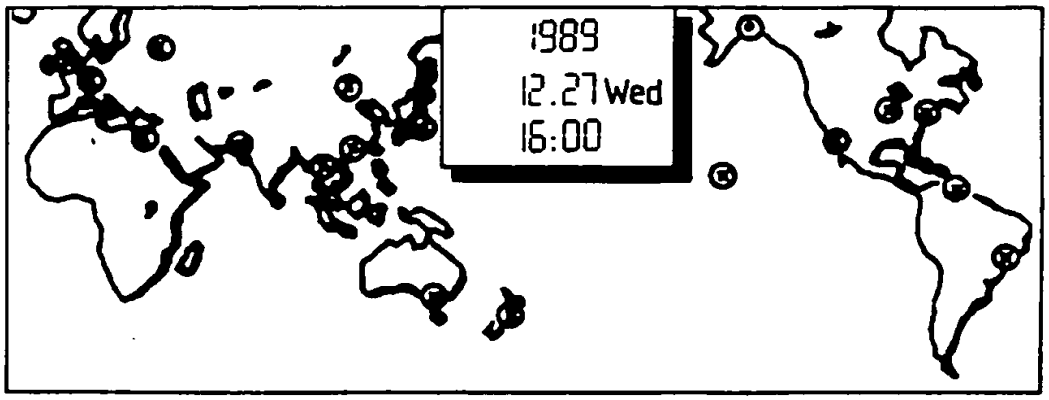


FIG. 12-1B

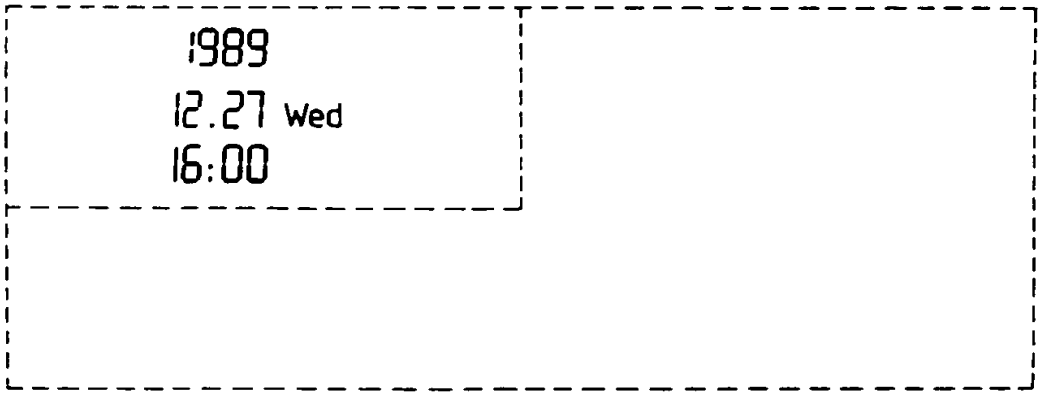


FIG. 12-2A

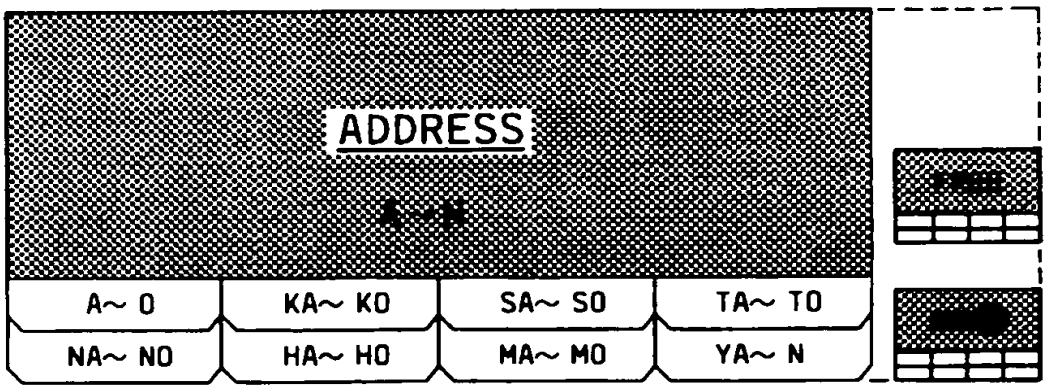


FIG. 12-2B

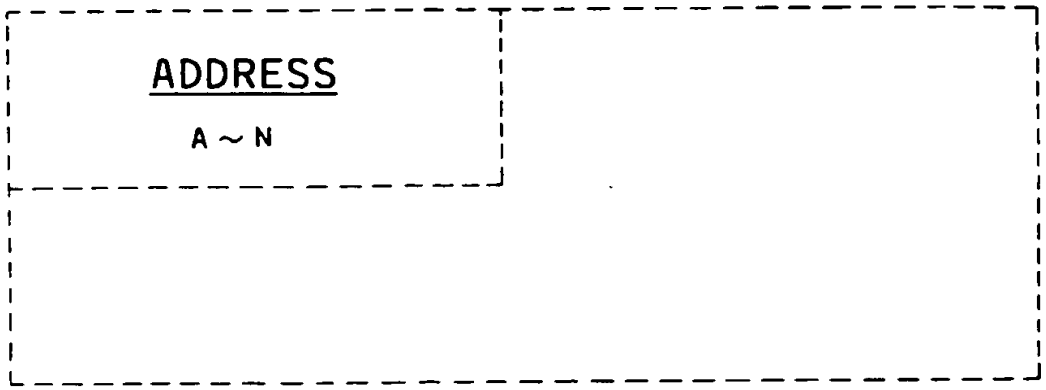


FIG. 12-3A

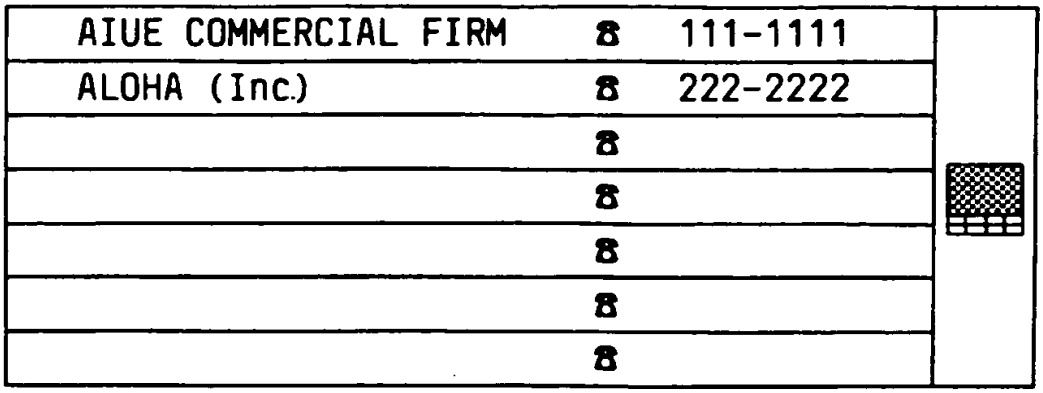


FIG. 12-3B

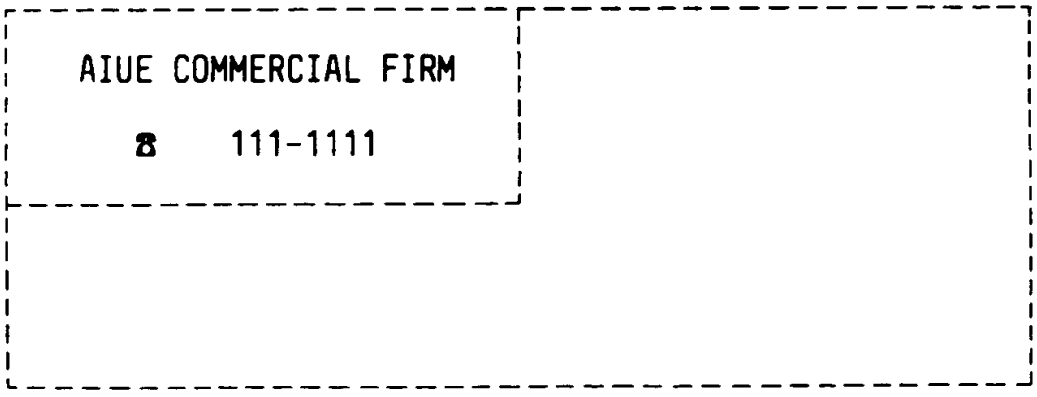


FIG. 12-4A

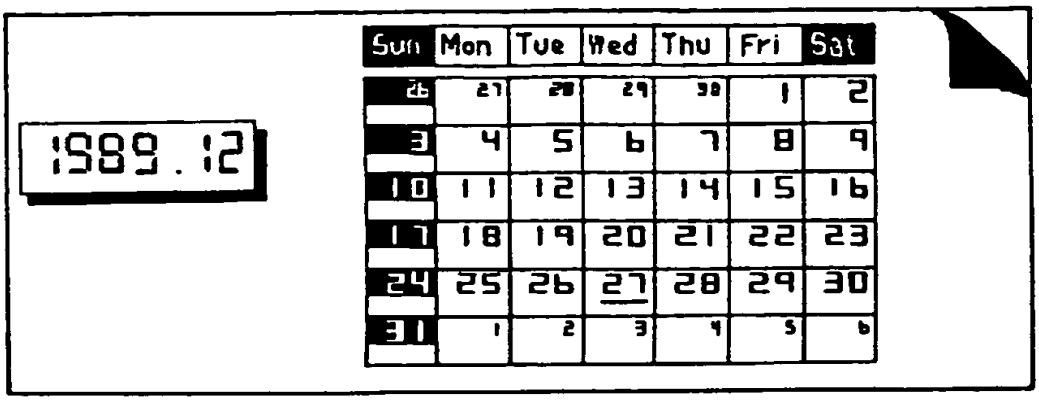


FIG. 12-4B

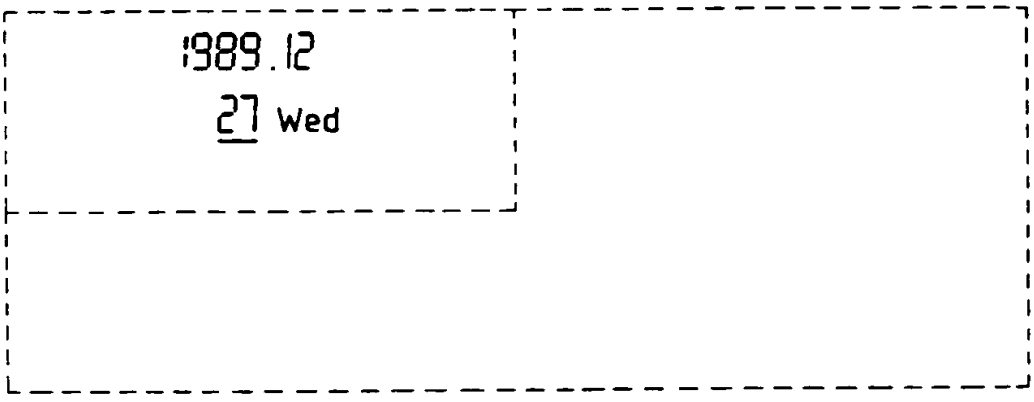


FIG. 12-5A

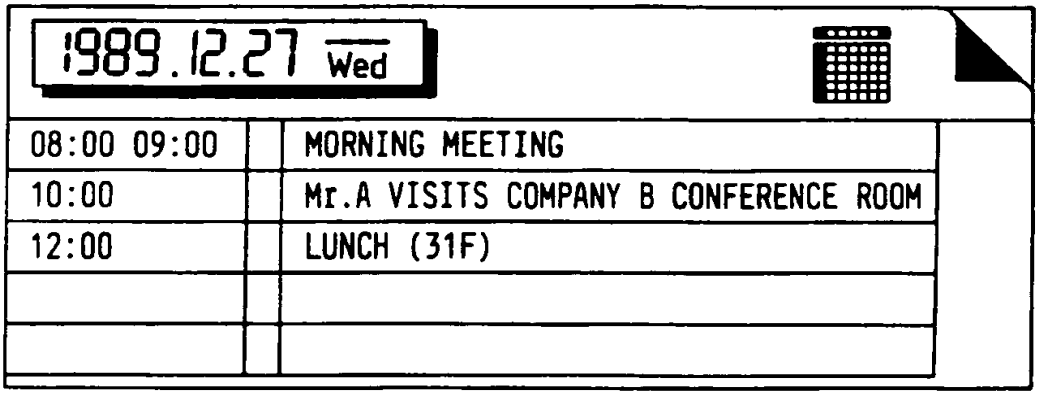


FIG. 12-5B

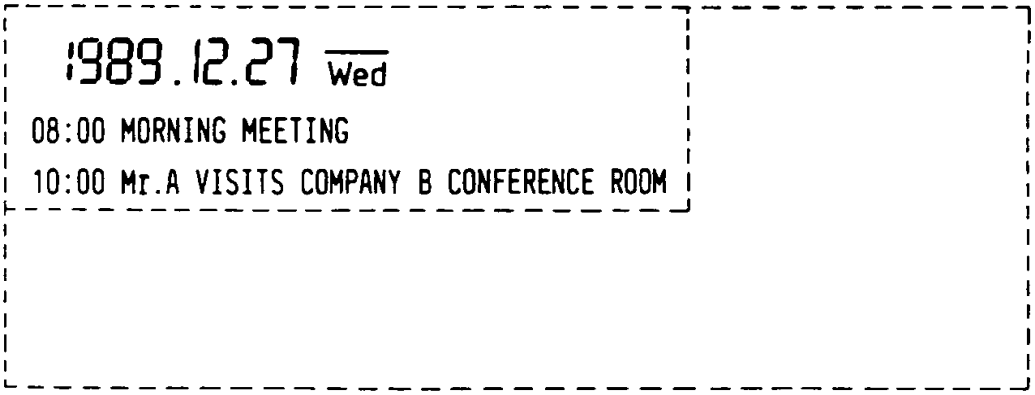


FIG. 13-1A

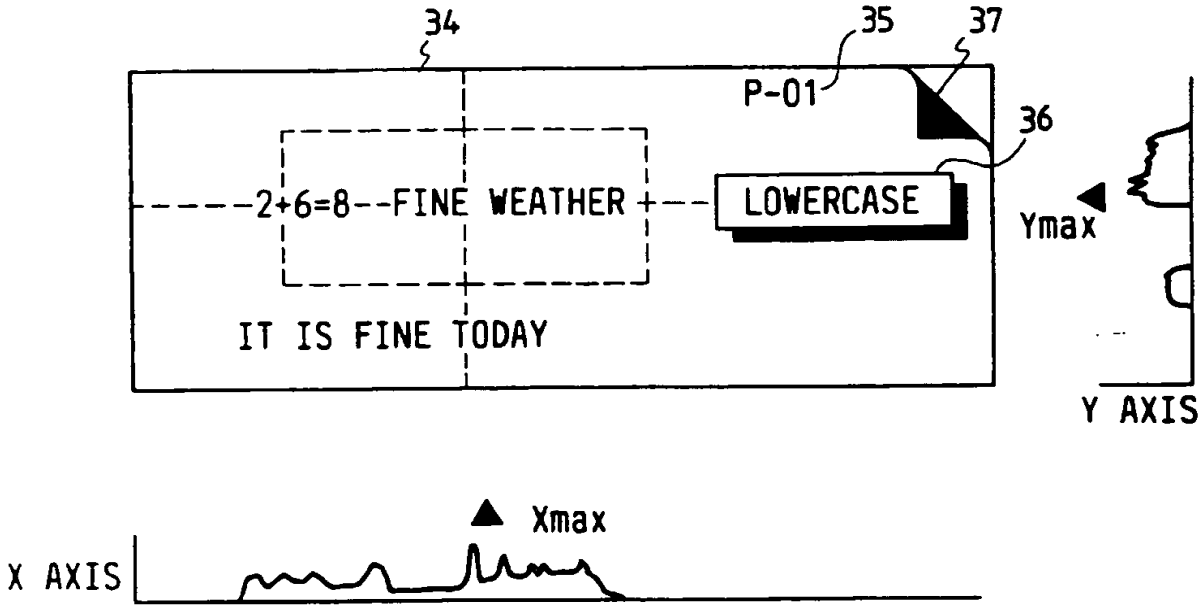


FIG. 13-1B

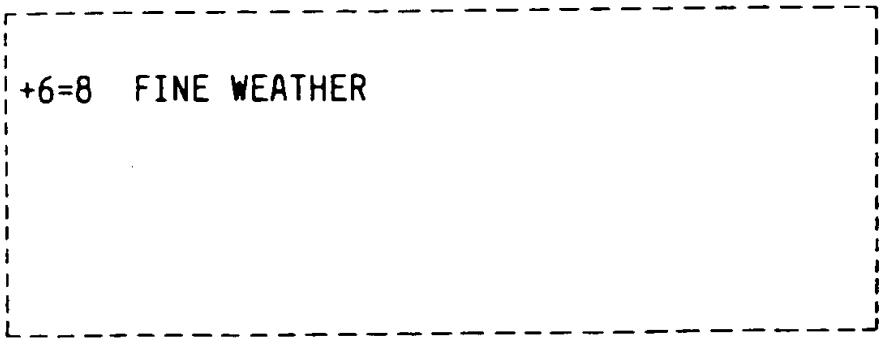


FIG. 13-2A

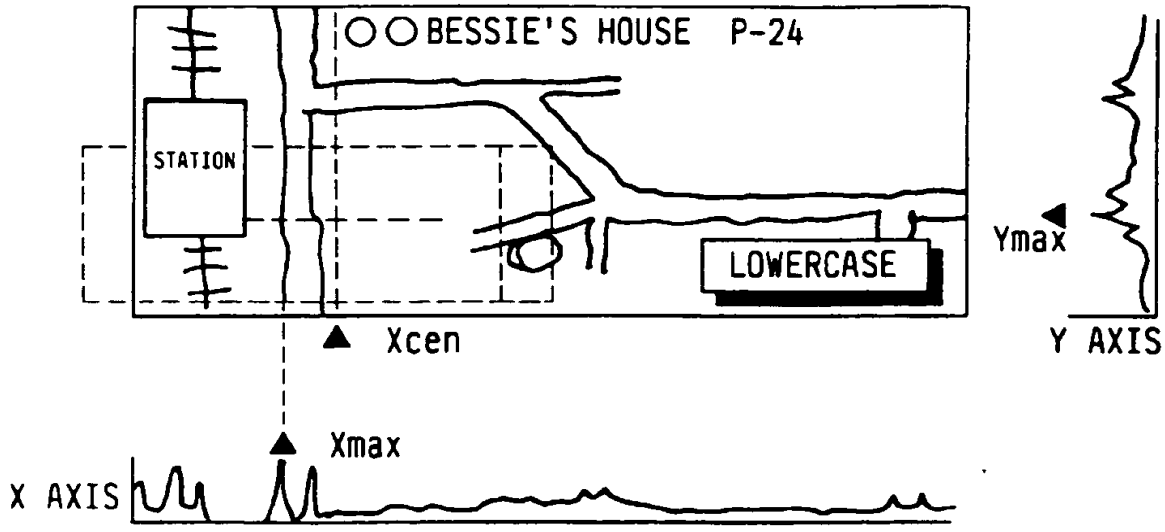


FIG. 13-2B

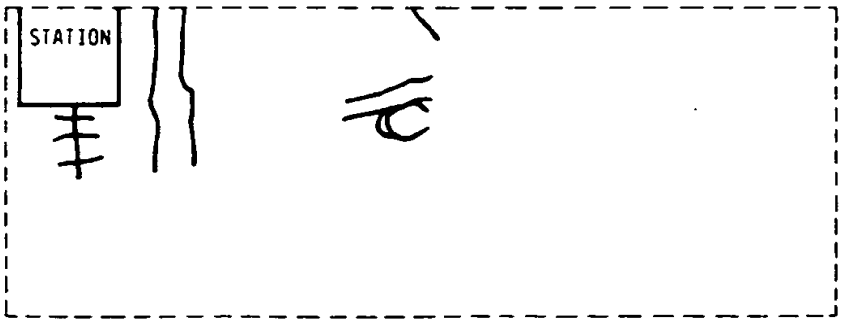


FIG. 14

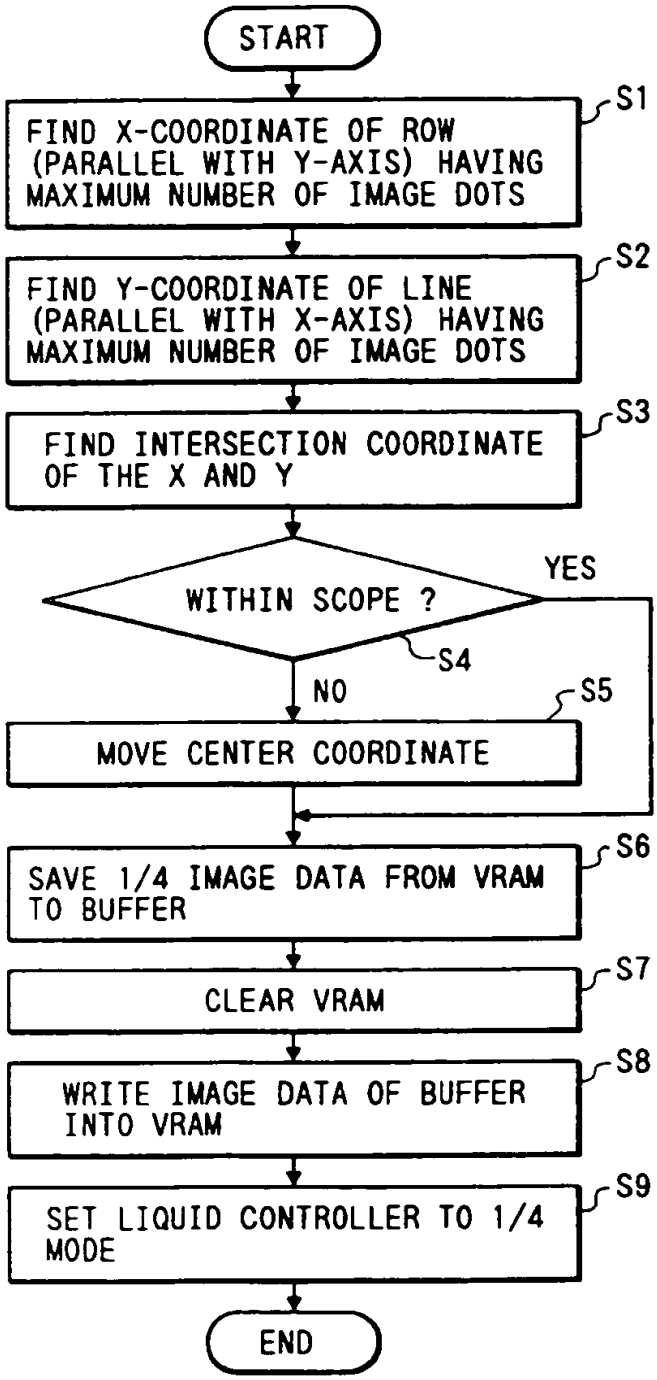

START
FIND X-COORDINATE OF ROW (PARALLEL WITH Y-AXIS) HAVING MAXIMUM NUMBER OF IMAGE DOTS
S1
FIND Y-COORDINATE OF LINE (PARALLEL WITH X-AXIS) HAVING MAXIMUM NUMBER OF IMAGE DOTS
S2
FIND INTERSECTION COORDINATE OF THE X AND Y
S3
WITHIN SCOPE ?
YES
S4
NO
S5
MOVE CENTER COORDINATE
SAVE 1/4 IMAGE DATA FROM VRAM TO BUFFER
S6
CLEAR VRAM
S7
WRITE IMAGE DATA OF BUFFER INTO VRAM
S8
SET LIQUID CONTROLLER TO 1/4 MODE
S9
END

FIG. 15A

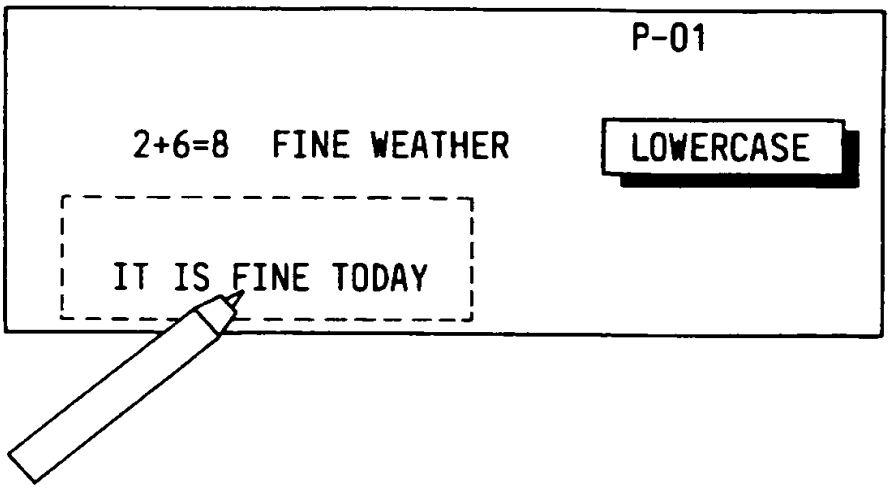
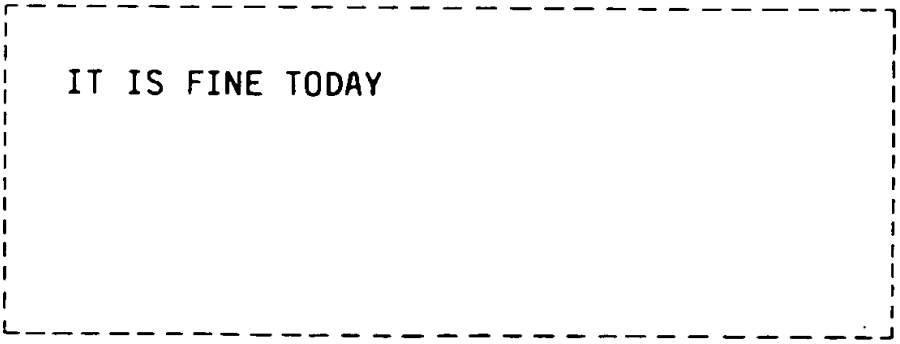


FIG. 15B



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